# ANALYSIS AND DESIGN OF 7T SENSE AMPLIFIERS IN 28 NM FD-SOI CMOS PROCESS

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ANÁLISE E PROJETO DE SENSOR AMPLIFICADOR TENSÃO 7T EM PROCESSO 28 NM FD-SOI CMOS

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O inesgotável esforço para se fabricar circuitos cada vez mais rápidos, de menor tamanho e com maior eficiência energética, fez com que efeitos nanométricos (< 90 nm) tenham que ser considerados no projeto destes circuitos. Devido a baixas tensões de alimentação, as clássicas equações de inversão forte para estimar a corrente de polarização e parâmetros de pequenos-sinais se tornam imprecisas, aumentando a complexidade na modelagem do projeto. Por outro lado, os processos de ponta FDSOI (Fully-Depleted Silicon on Insulator) podem reduzir consideravelmente as correntes de fuga e o descasamento dos transistores enquanto mantem a velocidade e robustez ao passo que consumo de energia seja extremamente reduzido para operações com tensões próximas da de *threshold*.

Esta tese se foca na análise operações em inversão moderada, desenvolvendo ferramentas para projetar o amplificador de tensão tipo latch de 7 transistores (7T-LTSA) em processo CMOS FDSOI de 28 nm. Adicionalmente, são propostos modelos compactos para o tempo de atraso do latch válidos para qualquer nível de inversão. Capacitâncias, transcondutâncias e condutâncias de canal de pequenos-sinais são analisadas e modeladas para fornecer uma equação compacta e de rápida avaliação. Por fim, uma figura de mérito (FoM) relacionando velocidade e desempenho é proposta. O consumo de energia é minimizado utilizando nível de tensão de alimentação próximo a tensão de *threshold*. Atraso abaixo de 100 ps é alcançado com $V_{DD}$=550 mV e abaixo de 1.5 ns com $V_{DD}$=350 mV apenas com dimensionamento correto dos transistores do 7T-LTSA, $\sigma_{off}$ é mantido abaixo de 18 mV para uma tensão de entrada diferencial igual a $0.1V_{DD}$ para $V_{DD}$ variando de 350 mV a 550 mV.

Abstract of Dissertation presented to COPPE/UFRJ as a partial fulfillment of the requirements for the degree of Master of Science (M.Sc.)

ANALYSIS AND DESIGN OF 7T SENSE AMPLIFIERS IN 28 NM FD-SOI CMOS PROCESS

Estêvão Fernandes de Lima Carvalho

February/2019

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The never ending strive to manufacture faster, smaller and energy efficient circuits, made several nanometric effects (< 90 nm) sizable and unavoidable for circuit design, such as severe mismatch variations, limited supply voltage levels, high leakage currents and several short-channel effects. Due to the low supply voltages used in these circuits, the classical strong inversion equations for bias currents and small-signal parameters turn out to be inaccurate, demanding more complexity to the model. On the other hand, state-of-art process such as FDSOI (Fully-Depleted Silicon on Insulator) can considerably reduce leakage currents and transistor mismatch while keeping speed and yield even with much lower energy consumption for operations centered around the moderate inversion region.

This thesis focuses on the analysis of transistors operating in moderate inversion, by developing tools for designing the classical latch-type sense amplifier with 7 transistors (7T-LTSA) for sub/near-threshold operations in a 28 nm FDSOI CMOS process. Compact models for the latch time delay valid for any inversion level will be presented, which are valid for $V_{DD}$=350 mV, 450 mV and 550 mV. Small-signal capacitances, transconductances and channel conductances are analyzed and modeled in order to provide compact and fast parameter evaluation. Lastly, a figure of merit (FoM) relating speed and yield is proposed. Energy consumption is minimized though the figure of merit at near-threshold supply voltage level. Time delay below 100 ps is reached with $V_{DD}$=550 mV and below 1.5 ns with $V_{DD}$=350 mV by proper transistor sizing of the 7T-LTSA, $\sigma_{off}$ is kept below 18 mV for a differential input voltage equals to $0.1V_{DD}$ for $V_{DD}$ ranging from 350 mV to 550 mV.

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# Chapter 1

# Introduction

The demand for faster, smaller and energy efficient system-on-chip (SoC) turned out to be a mandatory trend in digital circuit applications. In such scenario, CMOS latch-sense amplifiers (LTSAs) arise as an important circuit in digital applications, since LTSAs are widely used in SRAM (Static Random Access Memory) caches to read the data stored on memory cells [1]. It is also a fundamental block in many other applications such as analog-to-digital converters (ADCs) [2] and flip-flops (FFs) [3, 4].

The strong positive feedback of the LTSAs allows (Fig. 1.1) the amplification of differential signals at the required speed [5–7], however, mismatch variations can cause an incorrect signal amplification. One way to control mismatch variations, while keeping the same LTSA circuit topology, is by increasing the transistor area [8], however, large undesired capacitances can be produced. On top of that, circuit compactness forces maximum supply voltages to decrease since power dissipation must be reduced. In addition, the Internet of Things (IoT) trend led circuits to be driven by lower supply voltages. Either increasing transistor area or reducing supply voltage level can severely affect latch speed.

Latch sense amplifiers have been studied for decades and many works were reported providing good understanding on latch behavior [1, 9, 10]. In addition, several studies about the latch delay, differential input voltage offset and energy consumption were reported in literature [1, 9–15]. Among so many studies, this thesis focus on achieving the best compromise between energy consumption, yield and speed by filling two gaps:

**#1** To the best of our knowledge, analytical models of the latch delay can commonly be found linked to old SPICE models [1, 13], which neglects the smooth transition between weak and strong inversion, where the optimum energy vs. speed compromise in digital logic is commonly obtained [16, 17].

**#2** Compact equations for small-signal transconductance, capacitance and channel

conductance, which are valid from weak to strong inversion, to the best of our knowledge have not been reported yet. MOSFET models, such as BSIM [18], EKV [19] and PSP [20], include such parameters, however, for nanometric transistors, chart-based parameters are required for modeling short channel effects, making their equations only useful for circuit simulators [21].

## 1.1 The 7T-LTSA

The classical 7T-LTSA can be observed in Fig. 1.1. It comprises two cross-coupled CMOS inverters ($M_1$-$M_2$ and $M_3$-$M_4$), the tail transistor ($M_5$) and two switches ($M_6$ and $M_7$). The latch is connected to SRAM column bitlines denoted by $BL$ and $\overline{BL}$.

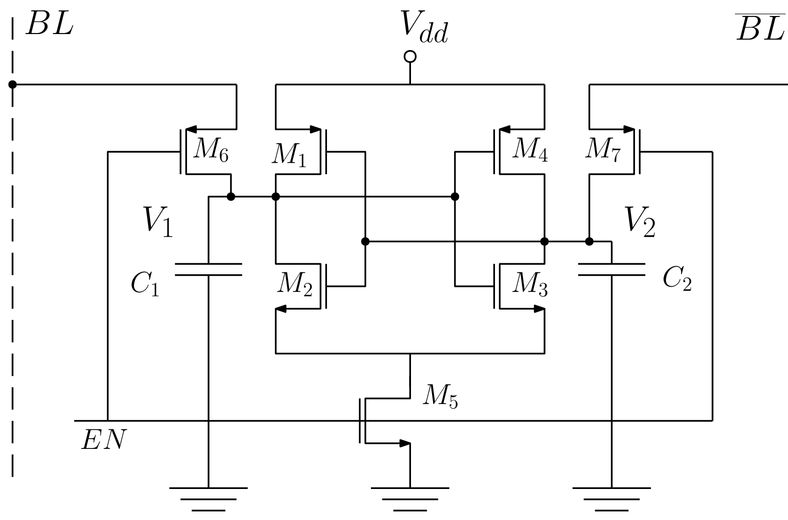


Figure 1.1: Schematic circuit of the 7T-LTSA.

During the off state ($EN = 0$ V), the switches $M_6$ and $M_7$ are turned on and $M_5$ is turned off. At this condition, the outputs $V_1$ and $V_2$ are directly connected to the SRAM bitlines $BL$ and $\overline{BL}$, respectively, and no decision occurs. On the other hand, during the on state ($EN = V_{DD}$), transistors $M_6$ and $M_7$ isolate the inverters from the bitlines ($V_1$ and $V_2$) and $M_5$ is enabled, thereby triggering the latch, which is composed by $M_1$, $M_2$, $M_3$ and $M_4$, and whose transient behavior is shown in Fig. 1.2.

The beginning of the transient decision illustrated in Fig. 1.2 starts with the internal nodes loaded with $V_1(0) = V_{indc} - V_{off}/2$ and $V_2(0) = V_{indc} + V_{off}/2$ where $V_{indc}$ and $V_{off}$ are the input common mode and differential mode voltages, respectively. At this point, both inverters push each other toward lower voltages [10]. Once an inverter output reaches the metastability value ($V_{S1}$ in Fig. 1.2), the positive feedback takes place, leading the inverter output voltage to 0, while the other

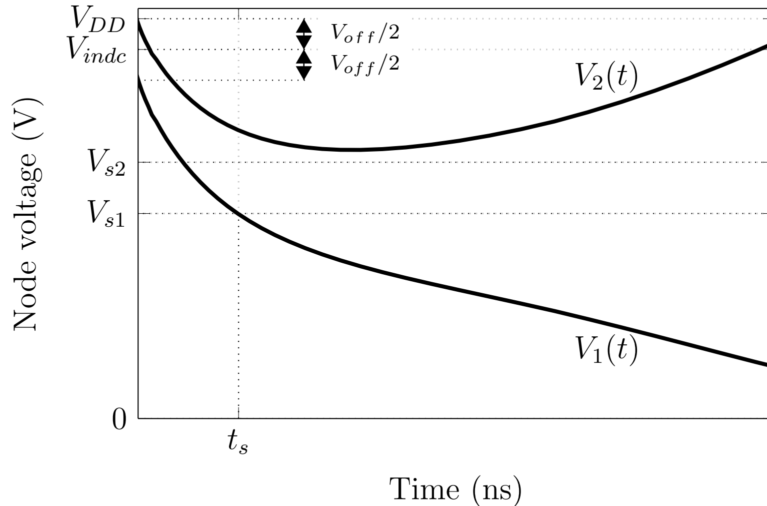


Figure 1.2: Transient behavior of the 7T-LTSA.

inverter output reaches $V_{DD}$. From now on, the inverter whose output converges to $V_{DD}$ will be called as *winner*, on the other hand, the inverter whose output converges to $GND$ will be called as *loser*.

### 1.1.1 Latch Performance Parameters

Latch performance comprises three parameters, as aforementioned, time delay, yield and energy consumption. Definitions of such parameters along with comments of what is considered acceptable in each case are presented next.

#### Delay Definition

Logic propagation robustness is strongly linked to noise margins [22]. For a correct decision, either the input signal must be higher than minimum high input voltage ($V_{IH}$) for a logic high, or must be lower than maximum low input voltage ($V_{IL}$) for a logic low (Fig. 1.3). To ensure correct decision, noise margins must be added to $V_{IH}$ and subtracted from $V_{IL}$ as a way of implementing a robust logic sense.

Adding noise margins to $V_{IH}$ and $V_{IL}$ may lead to very stringent safe logic levels. For many CMOS families, noise margins are designed to ensure "above safe" logic propagation [23]. A common and less stringent definition for the safe high threshold is $0.9V_{DD}$ and for the safe low threshold, $0.1V_{DD}$ [24]. From now on, delay is defined by the time that winner inverter takes to reach $0.9V_{DD}$ after the enable signal is set ($EN = V_{DD}$).

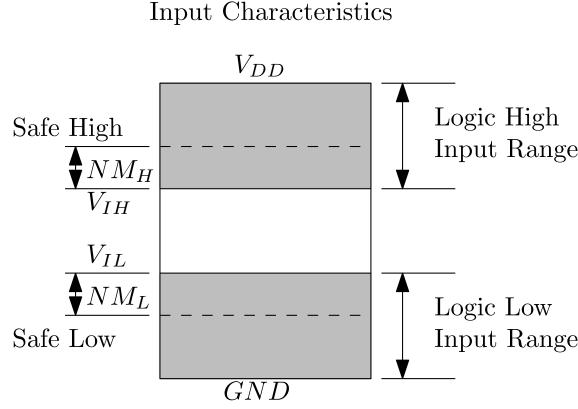


Figure 1.3: Static noise margins illustration.

### Yield Definition

For perfectly matched inverters, and for any given latch input differential voltage ($\Delta V_{in}$), the latch should be able to take the correct decision. Unfortunately, transistor mismatch shifts $V_{off}$ from the ideal 0 V to some voltage with higher magnitude. Nanometric technologies are severely affected by mismatch [21], therefore, circuit designers must run monte carlo simulations for evaluating latch decision robustness. The target parameter in such monte carlo simulations is called yield and defined by

$$Y = \frac{\text{number of correct decisions}}{\text{number of monte carlo samples}} \cdot 100 \tag{1.1}$$

which represents the percentage of correct decisions.

Yield is also the probability for the differential input voltage ($\Delta V_{in}$) to lie above $V_{off}$ [1]

$$Y(\Delta V_{in}) = P(V_{off} \leq \Delta V_{in}) \tag{1.2}$$

where the probability $P$ follows a gaussian distribution with standard deviation $\sigma_{off}$ and mean value $\mu_{off}$. The mean value $\mu_{off}$ is never 0, since the latch layout can never be perfectly symmetric due to the cross-coupled connections, demanding different metal layers. Nevertheless, can be made nearly negligible with proper layout techniques.

Once a proper estimate for $\sigma_{off}$ is obtained, the probability distribution is completely described. In order to obtain the yield value, the gaussian pdf is integrated from $-\inf$ to some offset voltage (Fig. 1.4), which gives

$$P(V_{off} \leq \Delta V_{in}) = \frac{1}{2} + \frac{1}{2}\text{erf}\left(\frac{\Delta V_{in}}{\sigma_{off}\sqrt{2}}\right) \tag{1.3}$$

where the function erf is the error function.

The number of incorrect decisions is also known in literature as bit error

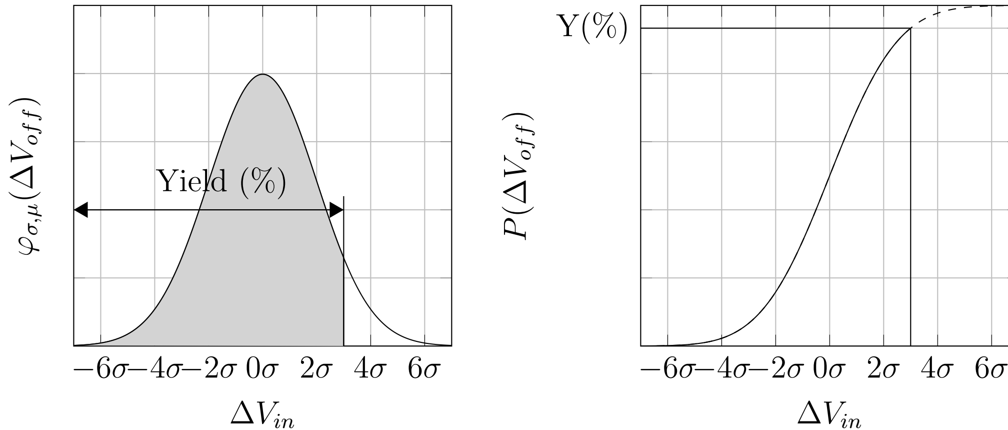


Figure 1.4: A gaussian probability density function (left) and its cumulative density function (right) defined in (1.3).

rate (BER) [25, 26], but both definitions essentially mean the same thing. BER ranges from $10^{-6}$ to $10^{-9}$ is usually satisfactory, which corresponds to, respectively, $\Delta V_{in}$=$5\sigma_{off}$ and $\Delta V_{in}$=$6\sigma_{off}$ in (1.3).

**Energy Consumption Definition**

Latch type comparators demand most power during decision lapse time ($P_{dyn}$), which is proportional to supply voltage level and inversely proportional to delay. In other words, the higher $V_{DD}$ is, the faster the decision is. This suggests that $P_{dyn}$ can be mainly improved in terms of $V_{DD}$ and delay.

The static leakage power is drawn even if no transient decision is triggered. Its sources arise from reverse bias *pn* junction leakage currents and tunneling currents, the latter are proportional to supply voltage levels. The total power dissipation is given by

$$P_{dissipation} = P_{leakage} + P_{dynamic}. \tag{1.4}$$

A commonly used figure of merit regarding the compromise between power dissipation and delay is called power-delay product (PDP) [27]. It is well known that the optimum PDP usually belongs to supply voltages levels about the threshold voltage of transistors in moderate inversion operations [11, 16, 17]. For supply voltages around 0.3 V, power consumption about a hundred of pico-watts can be found [15]. On the other hand, for supply voltages around 0.5 V and 0.6 V, power consumption is about some tenths of nanowatts to tenths of microwatts, respectively [15, 26].

## 1.2 Thesis Contribution

LTSAs have been under study for decades and the 7T-LTSA (Fig. 1.1) is the simplest LTSA structure. More sophisticated structures can improve the 7T-LTSA in speed, yield and energy consumption, in fact, many of then are worth noting e.g.: the sample boosted structure [28], the double-tail LTSA [3, 13], LTSA with pre-amplification stage [25], LTSA with post-amplification stage [7], among other topologies. However, the heart of so many architectures is the cross-coupled CMOS inverters, and in that sense, this work provides a tool for designers to obtain efficient solutions of the tradeoffs presented between speed, yield and energy from the cross-coupled CMOS inverters.

Since the scope of this work targets IoT applications, the first restriction will be energy consumption. As mentioned in beginning of this chapter and Sec. 1.1.1 this work uses supply voltages near the transistors threshold voltage, which implies in operation ranging from weak to moderate inversion. At this point we are left to face the two problems stated above and repeated here:

**#1** Analytical latch delay analysis can only be found linked to SPICE models, which neglects the smooth transition between weak and strong inversion.

**#2** Compact equations for small-signal transconductance, capacitance and channel conductance which hold from weak to strong inversion are nowhere to be found.

This work proposes solutions for the aforementioned problems by providing:

**Time delay equations for the CMOS latch regardless inversion level of operation:** In [1, 11, 13, 15, 29], expressions for latch delay are developed, however, the time models are imprecise in many points. First, coupling capacitance is usually not considered, which is comparable to load capacitance, and sometimes, might be even bigger. Second, latch regeneration phase is usually triggered by the pMOS transistor threshold voltage, which is never reached in sub-threshold operation. In Chapter 2, latch delay equations are developed including coupling capacitance and channel impedance. By eliminating threshold voltage dependent events, the developed equations are inversion level independent.

**Empirical compact equations for small-signal capacitances:** Accurate small-signal capacitance model is necessary in many circuit applications. Nevertheless, due to many short-channel effects, it is not possible to develop compact physical equations [21]. We start our analysis by noting that small-signal capacitance can be broken into intrinsic and extrinsic. On top of that, extrinsic can be further decomposed in overlap and fringe capacitances. Models for intrinsic, fringe

and overlap capacitances which can predict accurately measured data can be found [30–35]. Nonetheless, the inclusion of short channel effects results lengthy equations. This work uses the parallel composition of many small-signal capacitances and propose accurate and simple equations for gate-to-source, gate-to-drain, gate-to-body and junction capacitances.

**Empirical compact equation for small-signal transconductance:** MOSFET transconductance is a fundamental parameter in circuit analysis including but not limited to amplifiers, filters, RF devices and logic circuits [36]. A great effort has been taken in the last decades in order to model transistor behavior from weak to strong inversion operation. Compact transconductance equations were reported in literature [37–39]. Nevertheless, the different ways of current conduction through weak to strong inversion and short channel effects [21] forces the designer to work outside the region of validity of classical transconductance equations. In this work we propose a compact equation for transconductance based on the EKV model [38] as an explicit function of gate voltage. The proposed equation is more accurate than the classical one and holds from weak to strong inversion.

**Empirical/interpolated compact equation for small-signal channel conductance:** Few reported works have included $g_{ds}$ in CMOS latch circuit study. Channel conductance can be found in [40] where offset voltage is approached by studying the latch sampling phase (before decision). In [24] is reported a probabilistic study about metastability and noise which also includes $g_{ds}$. Both works [24, 40] point out the relevance of small-signal conductance, specially for small input voltages. In this work we propose an empirical/interpolated compact equation for small-signal channel impedance which holds from weak to strong inversion operation, and also takes into account short channel effects.

**Analytical figure of merit for CMOS latch including speed and yield:** The main objective of this thesis is to obtain an entirely analytical figure of merit that characterizes all the parameters of interest described so far. The proposed figure of merit is used for the 7T-LTSA design, the same design is carried out by circuit simulation, the resulting sense amplifiers are very similar, validating the proposed approach. The idea of obtaining an entirely analytical function for latch performance parameters arises from [1], where at the end of the article an elegant figure of merit which relates latch time delay and yield is proposed.

## 1.3 Thesis Outline

In Chapter 2 three different small-signal circuits of the latch dynamic response are developed. Equations for time delay are also advanced for each of small-signal models. The developed time delay models require a number of parameters which are presented in the following chapters.

Chapter 3 provides compact analytical equations for small-signal capacitances, transconductance and channel impedance. The provided equations arise from classical compact models, and some fitting parameters are added in order to keep the validity of the classical equations. This chapter uses the MATLAB routine developed [41], where a set of parameters were extracted for the transistor DC characteristics according to the EKV current equation [38, 42]. The aim of this chapter is to develop a MATLAB routine which will provide coefficients for the proposed quasi-static capacitances, transconductance and channel impedance equations of a 28 nm UTB FDSOI CMOS process. The parameters already provided by the routine developed in [41] are also delivered. Comparisons between the proposed equations and simulations using a 28 nm UTB FDSOI CMOS process are also presented in this chapter.

Chapter 4 presents the figure of merit relating time delay and input offset voltage. The proposed FoM is another perspective of the figure of merit from [1], where delay and offset are expanded to be functions of transistor width and transistor length on top of the differential input voltage. 7T-LTSA design guided by the proposed FoM in terms of input voltage offset and delay is provided. The results presented in this chapter are verified by simulations using the 28 nm UTB FDSOI CMOS process in the present work.

Concluding remarks and future directions are presented in Chapter 5.

# Chapter 2

# Delay Model

Latch delay is one of two major parameters accounted for LTSA performance. Many works can be found providing analytical approaches for latch speed [1, 12, 13, 40, 43–45], and in fact, for decades this subject has been severely studied. However, the short channel effects of nanometric technologies have spread in digital circuits pushing many effects, previously overlooked to the spotlight, leading to the point where secondary effects have become the major limiter. As a result, critical electric fields can be reached by no more than 1 V in many processes, leading to high leakage currents and power dissipation [46, 47]. In this scenario, lower supply voltages have become not only a way to keep technology scaling down, but a mandatory measure.

This chapter proposes compact equations for time delay estimation for three different latch models: ideal capacitor discharge model, capacitor discharge by coupled inverters model and capacitor discharge by coupled inverters including the channel conductance model. Each model adds more complexity, therefore, it expects to improve accuracy. The trade-off between speed and yield are evaluated in Chapter. 4.

## 2.1 Discharge and Regeneration Phases

Fig. 1.1 shows the 7T-LTSA schematic circuit. Its transient behavior is explained in Sec. 1.1. The term "latch decision" previously mentioned in Sec. 1.1 was introduced without any further elucidation. In [1], latch decision is described by the following events [1]:

- The $n$-type transistor of both inverters discharges the latch output nodes.
- One of the two inverters input voltage reaches $V_{DD} - V_{thp}$ first and its $p$-type transistor turns on, triggering the positive feedback.
- The $p$-type transistor regenerates the inverter output node to $V_{DD}$ while the $n$-type transistor of the other inverter never turns off, discharging its output

node to $GND$.

The chain of events aforementioned [1] is linked to the p-type transistor threshold voltage, therefore, unsuitable for sub-threshold operations.

In [10] we find a threshold voltage independent latch decision definition using the metastability voltage, $V_S$, as a trigger event for the positive feedback. The first inverter input to reach its metastability voltage value is the "loser" (output voltage goes to $GND$). In [15] an analysis of a regenerative latch using the bulk of a $p$-type transistor as input, Fig. 2.1, is carried on. Such latch operates in a similar manner as the latch under study (Fig. 1.1). The threshold event for guaranteed latch decision in [15] happens when the drain current ratio between $p$ and $n$-type of one inverter reaches 1, $I_{dp}/I_{dn} = 1$. From both definitions, latch transient decision events can be summarized as follows: both inverters discharge their output nodes until one of its input voltages reaches some value. Only then, the $p$-type which belongs to the "winner" draws from the supply voltage enough current to pull its output to $V_{DD}$.

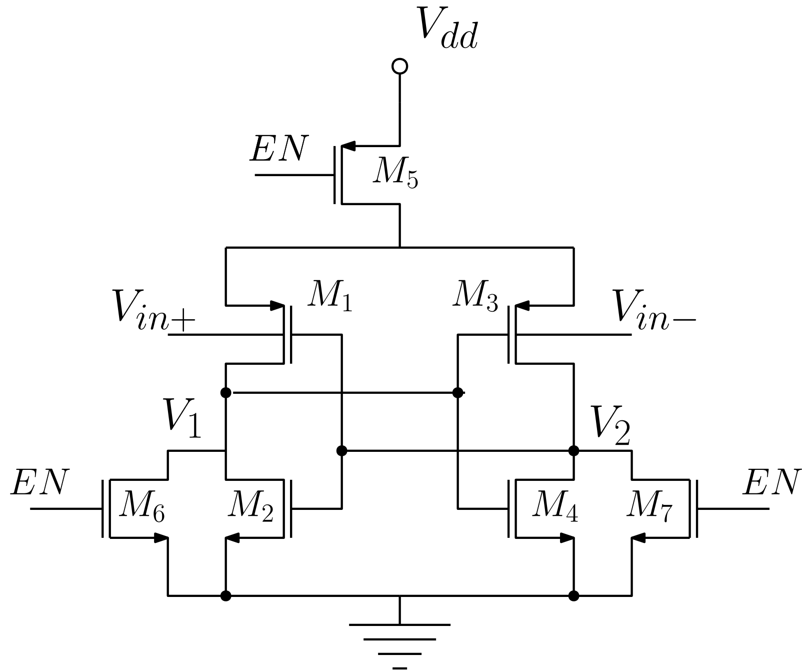


Figure 2.1: The 7T-LTSA regeneration mode.

From latch decision events described above, two phases can be distinguished from the winner inverter transient decision. One where the $n$-type transistor (that discharges the output node) is dominant, and other where the $p$-type transistor (that regenerates the output node) becomes the dominant transistor. Here, we propose a trigger event for dominant transistor change. Let the inverter composed by $M_4$ and $M_5$ in Fig. 1.1 be the winner. The time interval between the decision transient beginning and the time it takes for the loser inverter to reach its metastability voltage across the transient ($t_s$ in Fig. 2.2) is called discharging phase. The time

between the end of the discharging phase and the time it takes for the "winner" output to reach $0.9V_{DD}$ ($t_d$ in Fig. 2.2) is called the regeneration phase. The overall delay is given by

$$t_d = t_{discharge} + t_{regeneration} \tag{2.1}$$

where $t_{discharge}$ is the time interval from the transient beginning to the end of the discharging phase ($t_s$ in Fig. 2.2), and $t_{regeneration}$ is the time interval between the end of the discharging phase and the end of the regeneration phase ($t_d - t_s$ in Fig. 2.2).

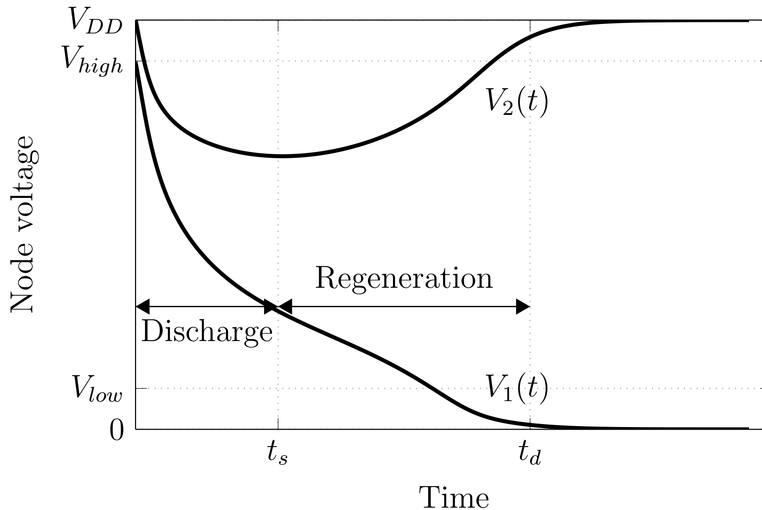


Figure 2.2: The two distinct phases in a latch decision transient.

In the next section, latch small-signal circuits around the metastability voltage value for three different 7T-LTSA models are advanced. Expressions for $t_s$ and the time difference between $t_d$ and $t_s$ are presented. The concept of discharging and regeneration phases introduces two different sets of effective parameters, which are shown to be necessary in order to accurately grasp the effects of both $n$ and $p$-type transistors during decision.

## 2.2 The Dynamic Model

We first consider the transistor small-signal model for both $n$ and $p$-type by connecting the source to bulk (Figs. 2.3 and 2.4, respectively). The schematic diagrams from Figs. 2.3 and 2.4 can be made clearer if $R_{ds}$ and $C_{jp}$ are replaced by their parallel impedance composition. The resulting schematic can be observed in Figs. 2.5 and 2.6. The resulting small-signal CMOS inverter composed by the $n$ and $p$-type from Figs. 2.5 and 2.6 is presented in Fig. 2.7.

Once again, since both $p$ and $n$-type transistor sources are bulk connected in small-signal analysis, many impedance blocks in Fig. 2.7 can be redrawn in a more

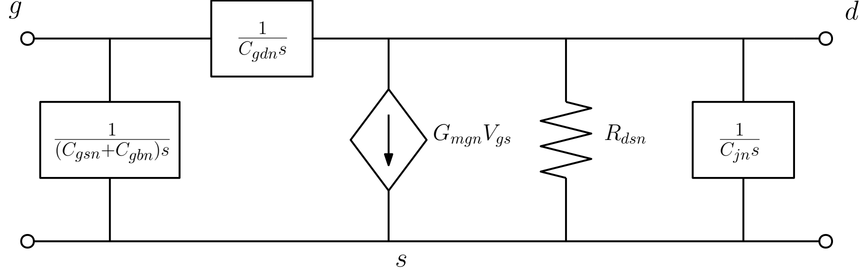


Figure 2.3: The $n$-type small-signal model.

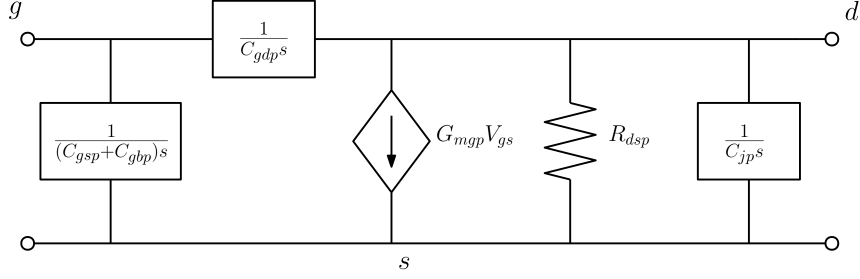


Figure 2.4: The $p$-type small-signal model.

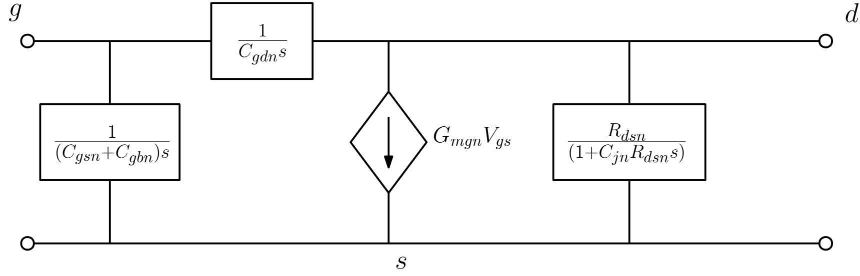


Figure 2.5: Compact $n$-type from Fig. 2.3.

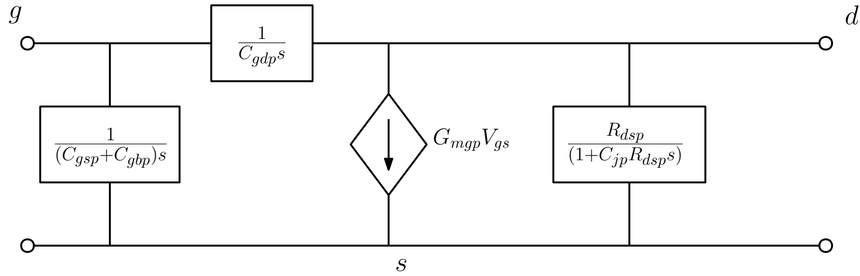


Figure 2.6: Compact $p$-type from Fig. 2.4.

compact way by their parallel composition. The resulting circuit is shown in Fig. 2.8.

If we connect two CMOS inverters in a cross coupled configuration we end up with the so called CMOS latch. Its small-signal circuit schematic is presented in Fig. 2.9. where $R_{ds1}$, $R_{ds2}$, $C_1$, $C_2$, $C_{c1}$, $C_{c2}$, $G_{m1}$ and $G_{m2}$ are given, respectively by

$$R_{ds1} = \frac{1}{g_{ds1}} \tag{2.2}$$

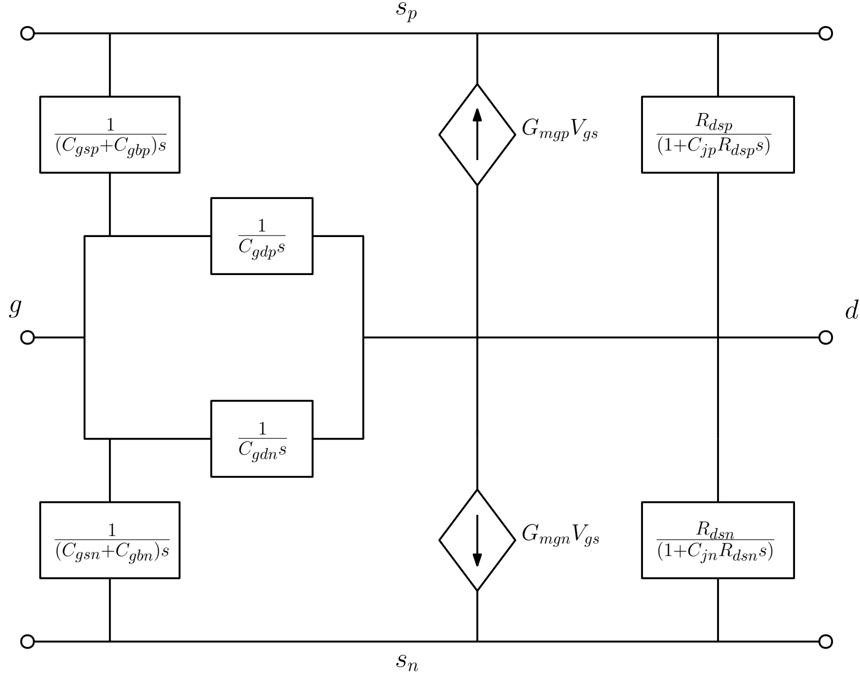


Figure 2.7: CMOS inverter small-signal model.

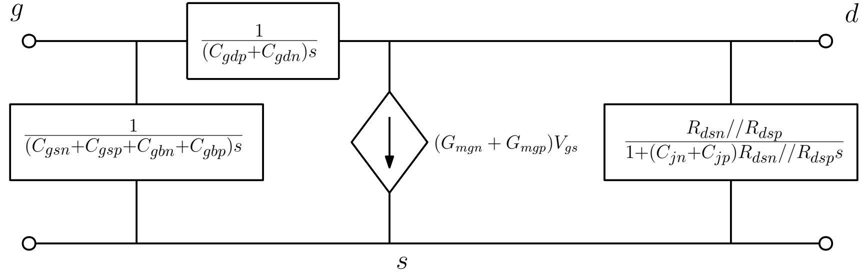


Figure 2.8: Compact CMOS inverter small-signal model from Fig. 2.7.

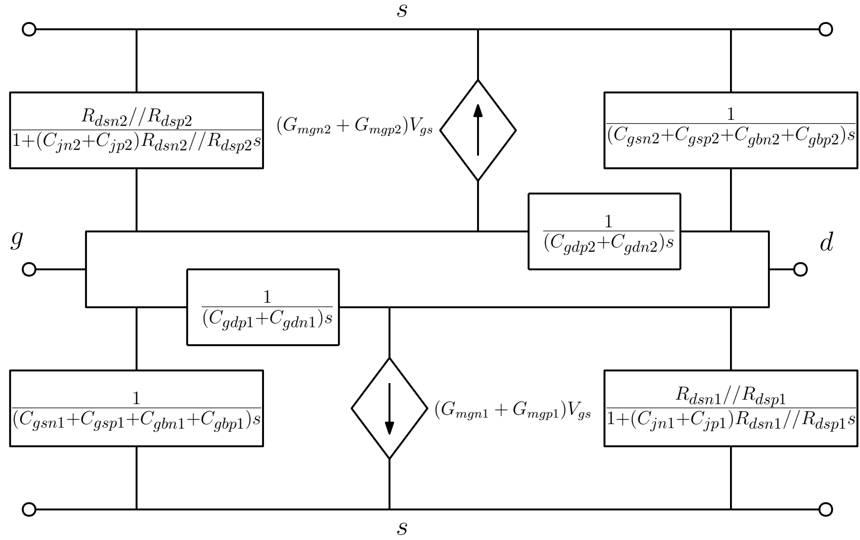


Figure 2.9: The latch small-signal model.

$$R_{ds2} = \frac{1}{g_{ds2}} \tag{2.3}$$

$$C_1 = C_{gsn2} + C_{gsp2} + C_{gbn2} + C_{gbp2} + C_{jn1} + C_{jp1} \tag{2.4}$$

$$C_2 = C_{gsn1} + C_{gsp1} + C_{gbn1} + C_{gbp1} + C_{jn2} + C_{jp2} \tag{2.5}$$

$$C_C = C_{gdn1} + C_{gdp1} + C_{gdn2} + C_{gdp2} \tag{2.6}$$

$$G_{m1} = G_{mgn1} + G_{mgp1} \tag{2.7}$$

$$G_{m2} = G_{mgn2} + G_{mgp2} \tag{2.8}$$

$$g_{ds1} = g_{dsn1} + g_{dsp1} \tag{2.9}$$

$$g_{ds2} = g_{dsn2} + g_{dsp2}. \tag{2.10}$$

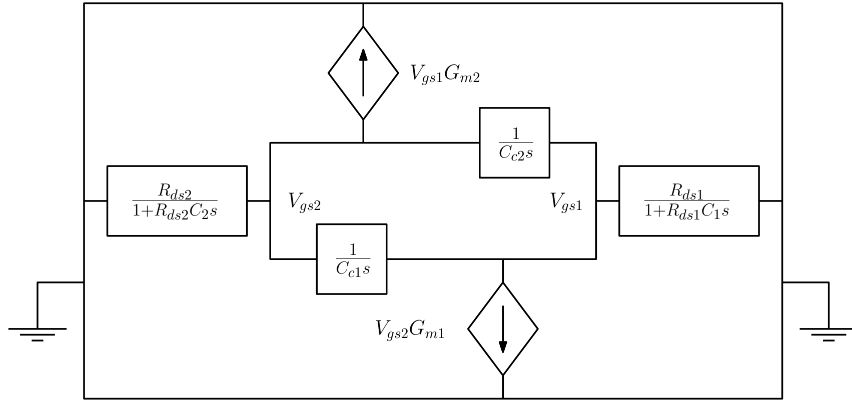


Figure 2.10: Compact latch small-signal model from Fig. 2.9.

The derived model in Fig. 2.9 can be observed in a more compact way in Fig. 2.10. Considering that the small-signal models derived are linearizations around each inverter metastability voltage, $V_{S1}$ and $V_{S2}$, we obtain the following dynamic equation system

$$\dot{V}_{gs1} = -\frac{G_{m1}}{C_c + C_1}(V_{gs2} - V_{S2}) + \frac{C_c}{C_c + C_1}\dot{V}_{gs2} - \frac{g_{ds1}}{(C_c + C_1)}(V_{gs1} - V_{S1}) \tag{2.11}$$

$$\dot{V}_{gs2} = -\frac{G_{m2}}{C_c + C_2}(V_{gs1} - V_{S1}) + \frac{C_c}{C_c + C_2}\dot{V}_{gs1} - \frac{g_{ds2}}{(C_c + C_2)}(V_{gs2} - V_{S2}). \tag{2.12}$$

A common simplification for the model given by (2.11) and (2.12) was reported in [9], which consists in neglecting the small-signal conductance. The resulting schematic can be found in Fig. 2.11 and the dynamic equations are given by

$$\dot{V}_{gs1} = -\frac{G_{m1}}{C_c + C_1}(V_{gs2} - V_{S2}) + \frac{C_c}{C_c + C_1}\dot{V}_{gs2} \tag{2.13}$$

$$\dot{V}_{gs2} = -\frac{G_{m2}}{C_c + C_2}(V_{gs1} - V_{S1}) + \frac{C_c}{C_c + C_2}\dot{V}_{gs1}. \tag{2.14}$$

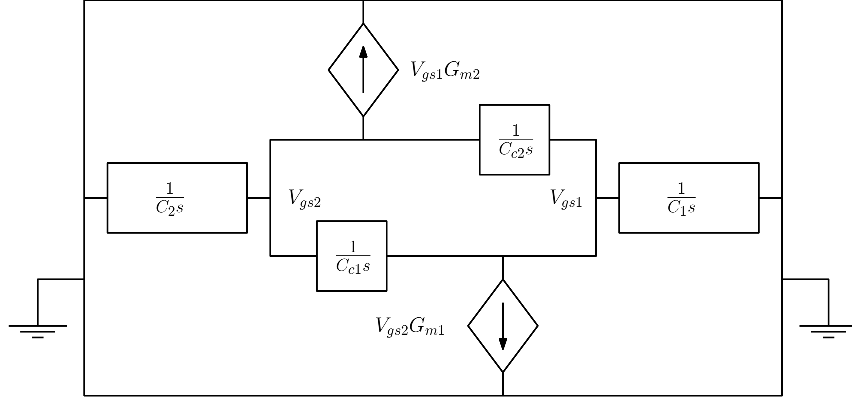


Figure 2.11: Compact latch small-signal model without channel resistance.

The most simplified latch model found in literature is presented in Fig. 2.12. Such small-signal circuit arises from further simplification of the schematic presented in Fig. 2.11 where coupling capacitance is neglected. The dynamic equation system is given by

$$\dot{V}_{gs1} = -\frac{G_{m1}}{C_1}(V_{gs2} - V_{S2}) \tag{2.15}$$

$$\dot{V}_{gs2} = -\frac{G_{m2}}{C_2}(V_{gs1} - V_{S1}). \tag{2.16}$$

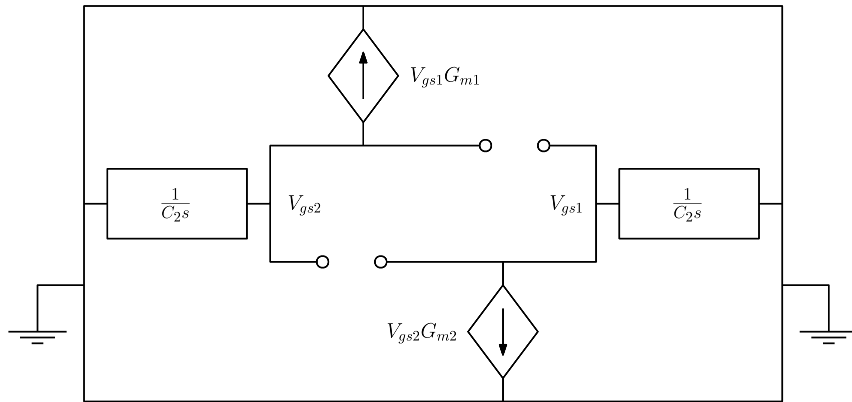


Figure 2.12: Compact latch small-signal model without coupling capacitance and output conductance.

Each set of dynamic equations has its relevance for instance, the most simplified ((2.15) and (2.16)) is used in a qualitative latch behavior analysis [9, 10, 48]. Coupling capacitance has a significant impact in digital logic delay [22], therefore, if a more accurate delay is desired, coupling capacitance is likely to be included ((2.13) and (2.14)). In fact, many works were reported studying offset input voltage and delay including coupling capacitance effects [9, 49, 50] nevertheless, channel conductance is usually overlooked in latch analysis. A probabilistic offset input

voltage study which includes conductance was reported in [24], nevertheless, to the best of our knowledge, a delay analysis including channel conductance has not been reported yet.

## 2.3 Time Analysis

Delay analysis and equations for all models presented in Sec. 2.2 are derived next.

### 2.3.1 The First Model

We start with the least complex model developed in Sec. 2.2, which is given by the schematic in Fig. 2.12. Assuming $C_1$=$C_2$=$C$, $G_{m1}$=$G_{m2}$=$G_m$ and $V_{S1}$=$V_{S2}$=$V_S$ and considering the initial conditions

$$V_1(0) = V_{indc} - V_{off}/2 \tag{2.17}$$

$$V_2(0) = V_{indc} + V_{off}/2 \tag{2.18}$$

we obtain

$$V_1(t) = (V_{indc} - V_S)\,\mathrm{e}^{-t\frac{G_m}{C}} - \frac{V_{off}}{2}\,\mathrm{e}^{t\frac{G_m}{C}} + V_S \tag{2.19}$$

$$V_2(t) = (V_{indc} - V_S)\,\mathrm{e}^{-t\frac{G_m}{C}} + \frac{V_{off}}{2}\,\mathrm{e}^{t\frac{G_m}{C}} + V_S. \tag{2.20}$$

Here we apply the concept of discharging and regeneration phases introduced in Sec. 2.1 into (2.19) and (2.20). We take advantage of the equations (2.19) and (2.20) by observing that both are composed by two exponential terms, a decaying one and an increasing one. We propose the effective parameters related to the discharging phase to be plugged in the decaying exponential time constant (denoted with subscript $\alpha$) and the effective parameters related to the regeneration phase to be plugged in the increasing exponential time constant (denoted with subscript $\beta$). Therefore, we rewrite (2.19) and (2.20) as

$$V_1(t) = (V_{indc} - V_S)\,\mathrm{e}^{-t\frac{G_{m\alpha}}{C_\alpha}} - \frac{V_{off}}{2}\,\mathrm{e}^{t\frac{G_{m\beta}}{C_\beta}} + V_S \tag{2.21}$$

$$V_2(t) = (V_{indc} - V_S)\,\mathrm{e}^{-t\frac{G_{m\alpha}}{C_\alpha}} + \frac{V_{off}}{2}\,\mathrm{e}^{t\frac{G_{m\beta}}{C_\beta}} + V_S. \tag{2.22}$$

As can be verified in Fig. 2.13, the decaying exponential is dominant during the discharging phase. On the other hand, the increasing exponential is dominant during regeneration phase.

Since the inverters are perfectly matched, the node whose voltage goes to $V_{DD}$, the "winner", is only determined by its initial condition. In view of the initial

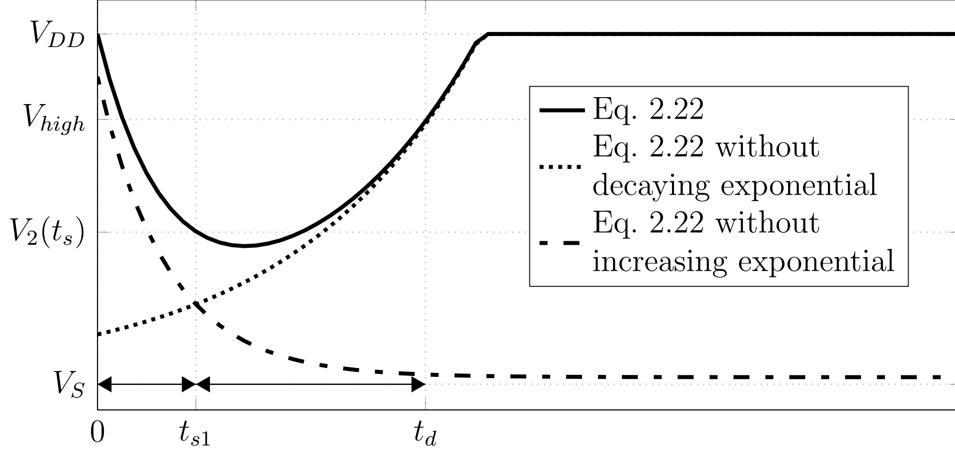


Figure 2.13: Dominant exponential behavior of (2.22). The figure was generated using (2.22) by best fit of the simulated behavior of a 7T-LTSA with $W_p$=240 nm, $W_n$=80 nm, $L_p$=$L_n$=30 nm and $V_{DD}$=0.5 V.

conditions (2.17) and (2.18), the node which goes to $V_{DD}$ is $V_2$ (Fig. 1.1), therefore, in order to obtain $t_{s1}$ we equal both exponential terms in (2.20) and find the time in which the decreasing exponential becomes no longer dominant. The result is given by

$$t_{s1} = \frac{C_\alpha C_\beta}{(C_\beta G_{m\alpha} + C_\alpha G_{m\beta})} \ln\left(2\frac{V_{indc} - V_S}{V_{off}}\right). \tag{2.23}$$

In order to calculate the regeneration phase time ($t_d - t_{s1}$ in Fig. 2.2), we approximate (2.20) to

$$V_2(t) = \frac{V_{off}}{2}\, \mathrm{e}^{t\frac{G_{m\beta}}{C_\beta}} + V_S \tag{2.24}$$

by dropping the decaying exponential term.

Such approximation can be verified to be fairly accurate for $t_d$ as can be observed in Fig. 2.13. Now we find $t(V_2)$ from (2.24)

$$t(V_2) = \frac{C_\beta}{G_{m\beta}} \ln\left(2\frac{V_2 - V_S}{V_{off}}\right). \tag{2.25}$$

Let the voltage at $t_d$ be the logical high threshold defined in Sec. 1.1.1 given by $0.9V_{DD}$, and the voltage at $t_{s1}$ be $V_2(t_{s1})$. The regeneration time, $t_d - t_{s1}$, can be found using (2.25), given by

$$t_d - t_{s1} = \frac{C_\beta}{G_{m\beta}} \left(\ln\left(2\frac{0.9V_{DD} - V_S}{V_{off}}\right) - \ln\left(2\frac{V_2(t_{s1}) - V_S}{V_{off}}\right)\right) \tag{2.26}$$

or

$$t_d - t_{s1} = \frac{C_\beta}{G_{m\beta}} \ln\left(\frac{0.9V_{DD} - V_S}{V_2(t_{s1}) - V_S}\right). \tag{2.27}$$

Consequently, the voltage $V_2(t_{s1})$ can be found by using (2.23) in (2.24)

$$V_2(t_{s1}) = (V_{indc} - V_S)\, \mathrm{e}^{\frac{G_{m\beta} C_\alpha}{(G_{m\beta} C_\alpha + G_{m\alpha} C_\beta)}} + V_S \tag{2.28}$$

which can be rewritten as

$$V_2(t_{s1}) = V_{exp\beta} + V_S \tag{2.29}$$

where $V_{exp\beta}$ is the increasing exponential value at $t_s$. Theoretically, the value of both decreasing and increasing exponentials at $t_s$ must be the same since $t_s$ is defined in such way. However, depending on how the effective parameters are defined, the value of both exponentials might not be the same. We propose to average both exponential terms in (2.22) in order to balance both $n$ and $p$-type transistor contributions at time $t_s$. Therefore, we define

$$\begin{aligned} \overline{V}_{exp1} = \frac{V_{exp\beta} + V_{exp\alpha}}{2} = \Bigg( & (V_{indc} - V_S)\, \mathrm{e}^{\frac{G_{m\beta} C_\alpha}{(G_{m\beta} C_\alpha + G_{m\alpha} C_\beta)}} \\ & + \frac{V_{off}}{2}\, \mathrm{e}^{\frac{G_{m\alpha} C_\beta}{(G_{m\beta} C_\alpha + G_{m\alpha} C_\beta)}} \Bigg) /2. \end{aligned} \tag{2.30}$$

where $\overline{V}_{exp1}$ is the average value of both the decaying and increasing exponentials at $t_s$ ($V_{exp\alpha}$ and $V_{exp\beta}$ respectively).

The delay equation for this model is the sum of both discharging phase delay (2.23) and regeneration phase delay (2.27), given by

$$t_d = \frac{C_\beta}{G_{m\beta}} \ln\left(\frac{0.9V_{DD} - V_S}{V_2(t_{s1}) - V_S}\right) + \frac{C_\alpha C_\beta}{(C_\beta G_{m\alpha} + C_\alpha G_{m\beta})} \ln\left(2\frac{V_{indc} - V_S}{V_{off}}\right). \tag{2.31}$$

One can ask why $t_d$ was not found directly by using (2.25). Since (2.25) is a weak function of the $n$-type transconductance, such approximation may be misleading for the case where the $p$-type drivability is much larger than the $n$-type.

### 2.3.2 The Second Model

Now we approach the latch small-signal model which comprises coupling capacitance (Fig. 2.11) given by the state equations (2.13) and (2.14). Solving (2.13) and (2.14) for the initial conditions, respectively, given by (2.17) and (2.18), and considering perfectly matched inverters, we obtain

$$V_1(t) = (V_{indc} - V_S)\, \mathrm{e}^{-t\frac{G_m}{C}} - \frac{V_{off}}{2}\, \mathrm{e}^{t\frac{G_m}{C + 2\,C_C}} + V_S \tag{2.32}$$

$$V_2(t) = (V_{indc} - V_S)\, \mathrm{e}^{-t\frac{G_m}{C}} + \frac{V_{off}}{2}\, \mathrm{e}^{t\frac{G_m}{C + 2\,C_C}} + V_S. \tag{2.33}$$

Once again, we stated that the decaying exponential is responsible for the discharging phase, on the other hand the increasing exponential is responsible for the regeneration phase, leading to

$$V_1(t) = (\,V_{indc} - \,V_S)\,\mathrm{e}^{-t\frac{G_{m\alpha}}{C_\alpha}} - \frac{V_{off}}{2}\,\mathrm{e}^{t\frac{G_{m\beta}}{C_\beta+2\,C_C}} + V_S \tag{2.34}$$

$$V_2(t) = (\,V_{indc} - \,V_S)\,\mathrm{e}^{-t\frac{G_{m\alpha}}{C_\alpha}} + \frac{V_{off}}{2}\,\mathrm{e}^{t\frac{G_{m\beta}}{C_\beta+2\,C_C}} + V_S. \tag{2.35}$$

If the state equations accounting for coupling capacitance, (2.32) and (2.33), are compared with (2.19) and (2.20), the only noticeable difference remains in the increasing exponential argument. Such effect unbalances the symmetry around the minimum voltage point and results in a transient behavior similar to Fig. 1.2.

Due to the initial conditions of the latch outputs, the inverter whose output node $V_2$ is the "winner". Therefore, we equate both exponential terms in (2.35) and find the explicit time when the decreasing exponential becomes no longer dominant. This leads to

$$t_{s2} = \frac{C_\alpha(C_\beta + 2C_C)}{((C_\beta + 2C_C)G_{m\alpha} + C_\alpha G_{m\beta})}\ln\left(2\frac{V_{indc} - V_S}{V_{off}}\right) \tag{2.36}$$

the subscript $\beta$ for $C_C$ in (2.32), (2.33) and (2.36) is unnecessary since it does not appear in the decaying exponential, thus not affecting the discharging phase.

We now apply the same approximation used in Sec. 2.3.1 by neglecting the decaying exponential in (2.33), in order to obtain $t_d - t_{s2}$, leading to

$$V_2(t) = \frac{V_{off}}{2}\,\mathrm{e}^{t\frac{G_{m\beta}}{C_\beta+2C_C}} + V_S. \tag{2.37}$$

We point out that such approximation is improved by the coupling capacitance effect as can be verified in Fig. 2.14, since the increasing exponential tends to slow down and provide more time for the decreasing exponential to become negligible.

Following the same steps developed in Sec. 2.3.1, we find the inverse function of (2.37), which is given by

$$t(V_2) = \frac{C_\beta + 2C_C}{G_{m\beta}}\ln\left(2\frac{V_2 - V_S}{V_{off}}\right). \tag{2.38}$$

Using (2.38) we find $t_d - t_{s2}$

$$t_d - t_{s2} = \frac{C_\beta + 2C_C}{G_{m\beta}}\left(\ln\left(2\frac{0.9V_{DD} - V_S}{V_{off}}\right) - \ln\left(2\frac{V_2(t_{s2}) - V_S}{V_{off}}\right)\right) \tag{2.39}$$

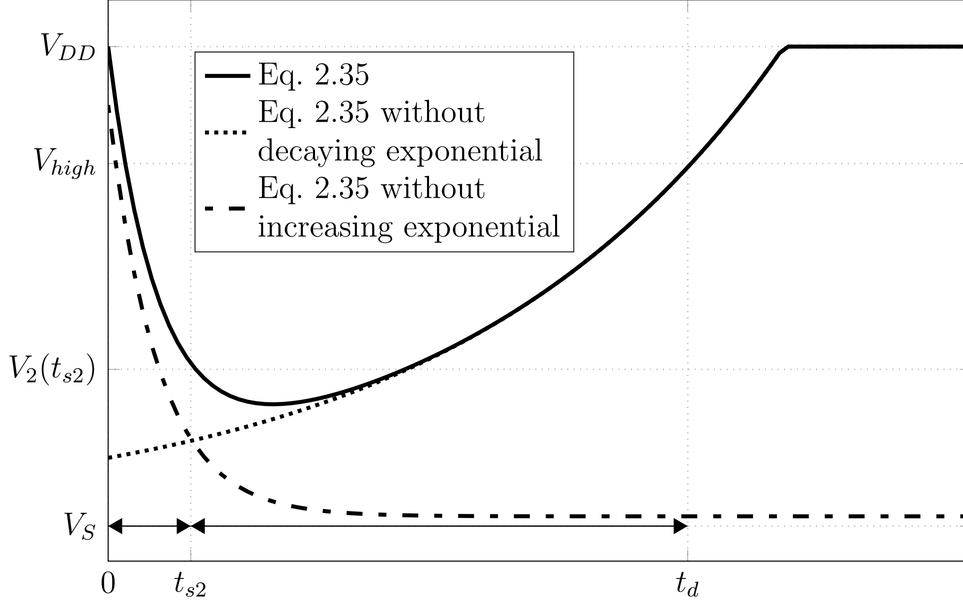


Figure 2.14: Dominant exponential behavior of (2.35). The figure was generated using (2.35) by best fit of the simulated behavior of a 7T-LTSA with $W_p$=240 nm, $W_n$=80 nm, $L_p$=$L_n$=30 nm and $V_{DD}$=0.5 V.

or

$$t_d - t_{s2} = \frac{C_\beta + 2C_C}{G_{m\beta}} \ln\left(\frac{0.9V_{DD} - V_S}{V_2(t_{s2}) - V_S}\right) \tag{2.40}$$

where $V_2(t_{s2})$ is defined as in (2.30) and given by

$$V_2(t_{s1}) = \overline{V}_{exp2} + V_S. \tag{2.41}$$

Now we find $\overline{V}_{exp}$ in (2.41) by taking the average of both exponentials in (2.35) at $t_{s2}$ and adding the inverter metastability voltage, $V_S$. The result is given by

$$\begin{aligned}\overline{V}_{exp2} = \Bigg( &(V_{indc} - V_S)\, \mathrm{e}^{\frac{G_{m\beta}C_\alpha}{(G_{m\beta}C_\alpha + G_{m\alpha}(C_\beta+2C_C))}} \\ &+ \frac{V_{off}}{2}\, \mathrm{e}^{\frac{G_{m\alpha}(C_\beta+2C_C)}{(G_{m\beta}C_\alpha + G_{m\alpha}(C_\beta+2C_C))}} \Bigg) /2.\end{aligned} \tag{2.42}$$

The delay equation for the model studied in this section is the sum of both discharging phase delay (2.36) and regeneration phase delay (2.40), given by

$$\begin{aligned}t_d = &\frac{(C_\beta + 2C_C)}{G_{m\beta}} \ln\left(\frac{0.9V_{DD} - V_S}{V_2(t_{s2}) - V_S}\right) \\ &+ \frac{C_\alpha(C_\beta + 2C_C)}{((C_\beta + C_C)G_{m\alpha} + C_\alpha G_{m\beta})} \ln\left(2\frac{V_{indc} - V_S}{V_{off}}\right).\end{aligned} \tag{2.43}$$

Comparing (2.31) and (2.43) one be observed differences in the constant multiplying the logarithmic functions. Such difference is expected to increase the time

delay with respect to (2.31). The effect of coupling capacitance, $C_C$, is sizable and is verified in Chapter 4.

### 2.3.3 The Third Model

The third model not only includes coupling capacitance, but channel conductance as well. The small-signal circuit can be observed in Fig. 2.10 and its state equations are given by (2.11) and (2.12). Solving such equations for the initial conditions given by (2.17) and (2.18), assuming perfectly matched inverters, the solution yields

$$V_1(t) = (V_{indc} - V_s)\,\mathrm{e}^{-t\frac{(G_m+g_{ds})}{C}} - \frac{V_{off}}{2}\,\mathrm{e}^{t\frac{(G_m-g_{ds})}{C+2\,C_C}} + V_S \tag{2.44}$$

$$V_2(t) = (V_{indc} - V_s)\,\mathrm{e}^{-t\frac{(G_m+g_{ds})}{C_\alpha}} + \frac{V_{off}}{2}\,\mathrm{e}^{t\frac{(G_m-g_{ds})}{C+2\,C_C}} + V_S. \tag{2.45}$$

We apply the same procedure used in Secs. 2.3.1 and 2.3.2 regarding both the discharging and regeneration phases and the effective parameters

$$V_1(t) = (V_{indc} - V_s)\,\mathrm{e}^{-t\frac{(G_{m\alpha}+g_{ds\alpha})}{C_\alpha}} - \frac{V_{off}}{2}\,\mathrm{e}^{t\frac{\left(G_{m\beta}-g_{ds\beta}\right)}{C_\beta+2\,C_C}} + V_S \tag{2.46}$$

$$V_2(t) = (V_{indc} - V_s)\,\mathrm{e}^{-t\frac{(G_{m\alpha}+g_{ds\alpha})}{C_\alpha}} + \frac{V_{off}}{2}\,\mathrm{e}^{t\frac{\left(G_{m\beta}-g_{ds\beta}\right)}{C_\beta+2\,C_C}} + V_S. \tag{2.47}$$

It can be verified that the unbalance between the exponentials in (2.32) and (2.33) is aggravated in (2.44) and (2.45) as well as the asymmetry around the minimum voltage point (Fig. 2.15).

We apply the same procedure used Sec. 2.3.1 and Sec. 2.3.2 in (2.47), in order to obtain $t_{s3}$, resulting in

$$t_{s3} = \frac{C_\alpha(C_\beta + 2C_C)}{((C_\beta + 2C_C)(G_{m\alpha} + g_{ds\alpha}) + C_\alpha(G_{m\beta} - g_{ds\beta}))} \ln\left(2\frac{V_{indc} - V_S}{V_{off}}\right). \tag{2.48}$$

Following the procedure used in Secs. 2.3.1 and 2.3.2, we neglect the decaying exponential in (2.47)

$$V_2(t) = \frac{V_{off}}{2}\,\mathrm{e}^{t\frac{(G_{m\beta}-g_{ds\beta})}{C_\beta+2C_C}} + V_S. \tag{2.49}$$

This approximation can be appreciated in Fig. 2.15. One can verify that it is, at least, as good as the same approximation for (2.37) since the effect of $g_{ds}$ aggravates the unbalance between both exponentials.

We now find the inverse function of (2.49), that is

$$t(V_2) = \frac{C_\beta + 2C_C}{(G_{m\beta} - g_{ds\beta})} \ln\left(2\frac{V_2 - V_S}{V_{off}}\right). \tag{2.50}$$

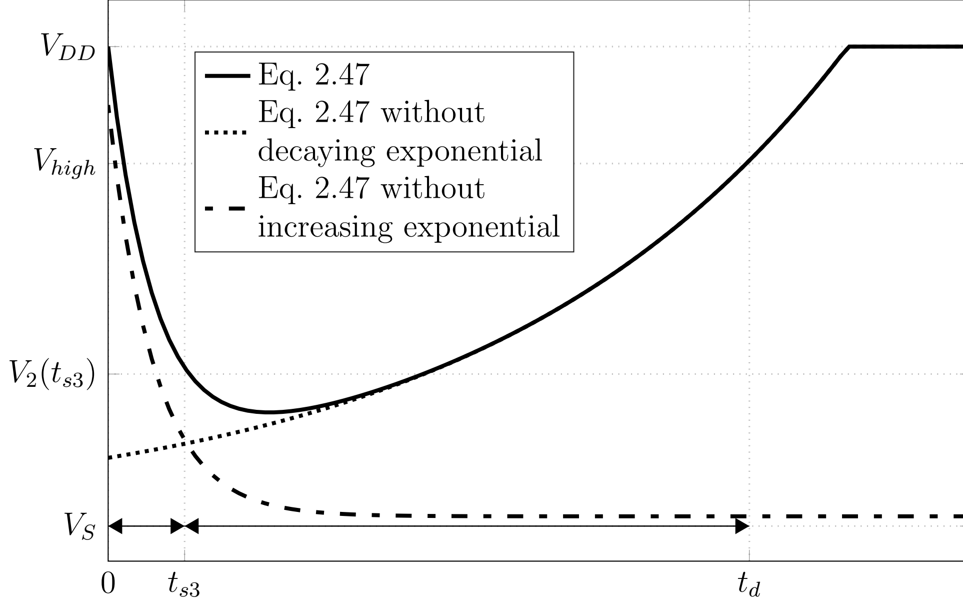


Figure 2.15: Dominant exponential change for (2.47). The figure was generated using (2.47) by best fit of the simulated behavior of a 7T-LTSA with $W_p$=240 nm, $W_n$=80 nm, $L_p$=$L_n$=30 nm, $V_{DD}$=0.5 V and $\Delta V_{in} = 50$ mV.

Using (2.50) we find $t_d - t_{s3}$

$$t_d - t_{s3} = \frac{C_\beta + 2C_C}{(G_{m\beta} - g_{ds\beta})} \left( \ln \left( 2\frac{0.9V_{DD} - V_S}{V_{off}} \right) - \ln \left( 2\frac{V_2(t_{s3}) - V_S}{V_{off}} \right) \right) \tag{2.51}$$

or

$$t_d - t_{s3} = \frac{C_\beta + 2C_C}{(G_{m\beta} - g_{ds\beta})} \ln \left( \frac{0.9V_{DD} - V_S}{V_2(t_{s3}) - V_S} \right) \tag{2.52}$$

where $V_2(t_{s3})$ is defined as in (2.30) and (2.41), given by

$$V_2(t_{s3}) = \overline{V}_{exp3} + V_S. \tag{2.53}$$

Now we find $\overline{V}_{exp3}$ in (2.53) using the same procedure used in Sec. 2.3.1 and Sec. 2.3.2. The result is given by

$$\begin{aligned} \overline{V}_{exp3} = \Bigg( & \left( V_{indc} - V_S \right) \mathrm{e}^{\frac{(G_{m\beta} - g_{ds\beta})C_\alpha}{((G_{m\beta} - g_{ds\beta})C_\alpha + (G_{m\alpha} + g_{ds\alpha})(C_\beta + 2C_C))}} \\ & + \frac{V_{off}}{2} \mathrm{e}^{\frac{(G_{m\alpha} + g_{ds\alpha})(C_\beta + 2C_C)}{((G_{m\beta} - g_{ds\beta})C_\alpha + (G_{m\alpha} + g_{ds\alpha})(C_\beta + 2C_C))}} \Bigg). \end{aligned} \tag{2.54}$$

The delay equation for the model including both coupling capacitance, $C_C$, and channel impedance, $g_{ds}$, is the sum of both discharging phase delay (2.48) and

regeneration phase delay (2.52), given by

$$t_d = \frac{(C_\beta + 2C_C)}{(G_{m\beta} - g_{ds\beta})} \ln\left(\frac{0.9V_{DD} - V_S}{V_2(t_{s3}) - V_S}\right) + \frac{C_\alpha(C_\beta + 2C_C)}{((C_\beta + C_C)(G_{m\alpha} + g_{ds\alpha}) + C_\alpha(G_{m\beta} - g_{ds\beta}))} \ln\left(2\frac{V_{indc} - V_S}{V_{off}}\right). \tag{2.55}$$

## 2.4 Summary

An alternative description, threshold independent, for latch decision transient was introduced in Section 2.1. In Section 2.2, three different sets of state equations, which governs the zero-input[1] latch transient response, were developed in a step-by-step way. Such equations were derived in Section 2.3, where time delay equations were derived for the CMOS latch valid in all inversion levels of operation. The proposed equations are fully dependent on transistor transconductance, capacitances, conductance and inverter metastability voltage. Simulations validating the latch time delay models developed are presented in Chapter 4.

[1] Dynamic system only governed by the initial conditions [51]

# Chapter 3

# $C$, $G_m$ and $g_{ds}$ Models

The effective parameters introduced in Section 2.2 are only approximations for the actual values of the transconductances, capacitances and channel conductance. In fact, choosing an effective parameter usually means picking the best value which fits some characteristic curve. Sometimes, such procedure may take away the physical meaning from the fitted parameter for example, if the effective $G_m$ is obtained by fitting some extracted characteristic curve, transistor width and length effect on $G_m$ might be hidden. For the scope of this work, the consideration of the effective parameters as functions of transistor width and length has primary importance.

In this chapter, we advance a study for the transistor transconductance, capacitance and channel conductance, investigating how both transistor sizing and bias conditions affect the value of such parameters in the 28 nm UTB FDSOI CMOS process. The proposed equations are developed to hold regardless the process, therefore they can be adequately adapted to another CMOS process.

The remainder of this chapter is divided in four sections. Sections 3.1, 3.2 and 3.3 are dedicated to the development of analytical models for small-signal capacitances, transconductance and channel conductance. Short-channel effects are considered in the proposed equations. Extensive simulations are carried out in order to verify that the proposed models hold for a large range of transistor sizes and bias voltages. Concluding remarks are made in Section 3.4.

## 3.1 Capacitances

A successful model for MOSFET small-signal capacitance is mandatory for accurate prediction of any transistor AC characteristic. RF applications demand accurate non-quasi-static models, which leads to complex small-signal elements only useful for computer simulation. Since the scope of this work belongs to digital applications, we limited out analysis from stepping in the RF territory, hence, the proposed models should not be used for beyond quasi-static region [21].

MOSFETs can be viewed as a composition of $pn$ junctions namely, source-to-bulk, drain-to-bulk and channel-to-bulk junctions furthermore, the gate-to-bulk junction depletes as well. On top of that, gate, source, drain and bulk interact with each other through the channel [21] hence, even for quasi-static small-signal models, many elements are comprised in the linearized circuit.

A classical definition of transistor upper frequency limit of operation given by

$$\omega_0 = \frac{\mu(V_{GS} - V_T)}{\alpha L^2} \tag{3.1}$$

suggests that the maximum frequency increases with supply voltage and mobility and decreases with transistor length [21, 38]. Although $V_{DD}$ (consequently, $V_{GS}$) is very limited in the scope of this work ( $< 1$ V), mobility is expected to be high for state-of-art processes . Also playing in favor of raising the upper frequency limit, transistor length is becoming smaller and smaller every generation, extending the quasi-static model frequency limit of validity.

### 3.1.1 Load and Coupling Capacitance Breakdown

The compositions of both load and coupling capacitances are given by (2.4), (2.5) and (2.6). Their composition in terms of transistor parasitics can be observed in Figs. 2.3, 2.4, 2.5, 2.6, 2.7, 2.8 and 2.9, however, for clarification, we have redrawn the set of capacitances that compose the load ($C_1$ and $C_2$) and coupling ($C_C$) capacitances of the 7T-LTSA in Fig. 3.1. Because the several parasitics are in parallel, load and coupling capacitances can be rewritten as

$$C_1 = C_{gsn2} + C_{gsp2} + C_{gbn2} + C_{gbp2} + 2C_{jp1} + C_{jn1} \tag{3.2}$$

$$C_2 = C_{gsn1} + C_{gsp1} + C_{gbn1} + C_{gbp1} + 2C_{jp2} + C_{jn2} \tag{3.3}$$

$$C_C = C_{gdp1} + C_{gdn1} + C_{gdp2} + C_{gdn2} \tag{3.4}$$

where the extra $p$-type junction capacitance in comparison with (2.4), (2.5) arises from the pass gate transistor connected to the bitlines ($M_6$ and $M_7$ in Fig. 1.1), not accounted for in (2.4) and (2.5).

In order to estimate load and coupling capacitances, the procedure suggested in [33, 52] was applied in both $p$ and the $n$-type transistors. Simulations carried out for extraction of each capacitance are described in detail in the following subsection. For clarification, we state some facts and assumptions about the small-signal circuit to simplify the capacitance model:

- Capacitances $C_{gs}$, $C_{gd}$ and $C_{gb}$ have both intrinsic and extrinsic parts which are connected in parallel [21].

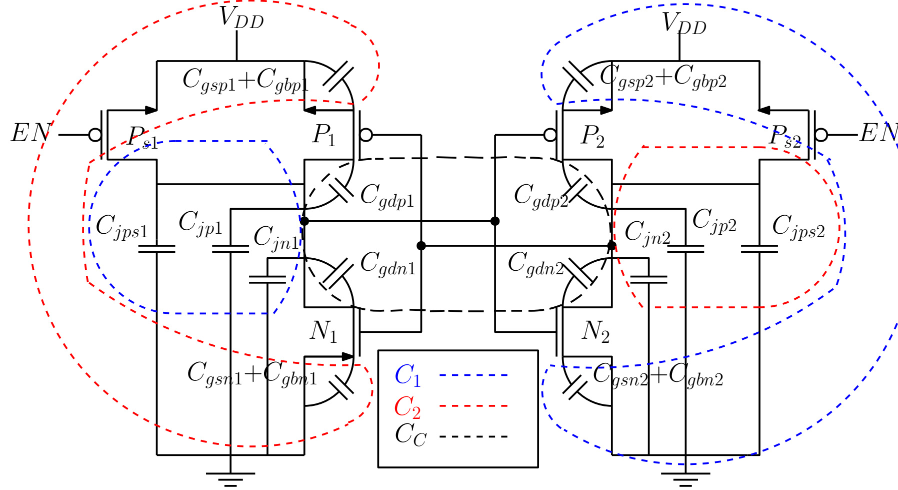


Figure 3.1: 7T-LTSA capacitances that have influence on the dynamic behavior.

- Both $p$ and $n$-type transistors have source and bulk connected, therefore, gate-source capacitance is in parallel with $C_{gb}$ (Fig. 3.2) and bulk-source capacitance is 0.
- Bulk-drain capacitance are neglected.
- Channel charge distribution is strongly affected by bias conditions. Gate poly and source (and drain) junction depletion are also affected by bias, however, assumed to be much weaker in comparison with the channel depletion.
- $C_{ds}$ is not included in fact, for quasi-static models, its effect is usually neglected [21].

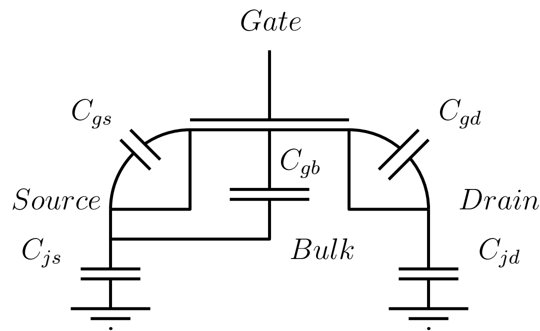


Figure 3.2: Transistor small-signal capacitors responsible for the latch dynamics as stated.

In the following subsection, analytical models are advanced, along with parameter extraction for each proposed equation.

### 3.1.2 $C_{gs}$ and $C_{gd}$ Model

In Fig. 3.3 the $C_{gs}$ behavior of the $n$-type regular $V_T$ for various widths and two different biases can be appreciated. Observe that both graphs are strongly affected by the bias change. This can be explained by the channel formation due to inversion and the channel charge modulation due to saturation. The lack of charges in the channel (characteristic of deep-weak inversion behavior) leads to very small charge variation when biases are varied ($V_{GS} \leq 0.2$ V for $V_{DS}$=100 V and $V_{GS} \leq 0.4$ V for $V_{DS}$=320 V), causing low small-signal capacitance. On top of that, once the transistor becomes pinched off, channel charge turns out to be independent of drain voltage, while the source region control over the channel increases. Both effects contributes to $C_{gs}$ increase with $V_{GS}$ note that larger $V_{DS}$ shifts the $C_{gs}$ ramp up regarding to $V_{GS}$.

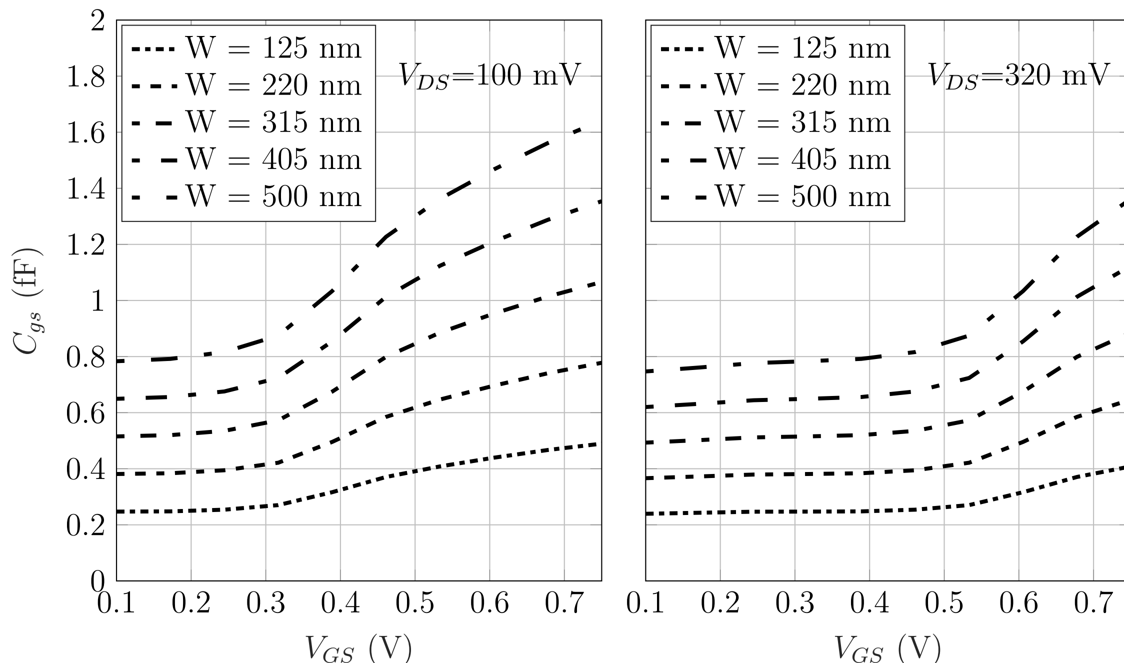


Figure 3.3: $C_{gs}$ obtained using a 28 nm UTB FDSOI CMOS process. Simulation was carried out for the $n$-type regular $V_T$ with $L$=30 nm.

In order to model the behavior observed in Fig. 3.3, we decomposed $C_{gs}$ into intrinsic and extrinsic capacitances. Extrinsic capacitance arises from the overlap and fringing fields between gate and diffusion of the source or drain regions (Fig. 3.4). A good model for overlap capacitance for MOS devices can be found in [35]. Fringing capacitance for SOI devices is modeled in [34]. Both studies do not take bias conditions into account, which can affect extrinsic capacitances through source (or drain) region depletion, gate poly depletion [21] and oxide degradation due to hot carriers [53]. However, as mentioned in Sec. 3.1.1, bias effects are far more severe in the intrinsic component than in extrinsic, so we assume that intrinsic capacitance

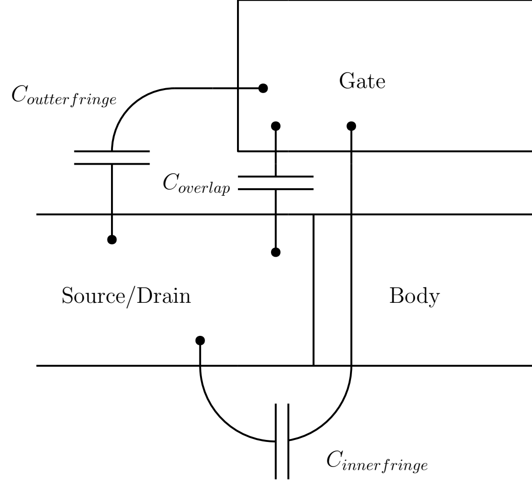


Figure 3.4: Composition of source (drain) extrinsic capacitance.

accounts for all bias effects, while extrinsic capacitance is bias independent.

Intrinsic capacitance dependency with bias is continuously defined in classical current-based models [38, 39]. For simplicity, we developed a model assuming transistor saturation and propose an empirical change to deal with the intrinsic capacitance ramp up. We start with the intrinsic gate-to-source capacitance found in [21] and given by

$$C_{gs_{intrinsic}} = WLC_{ox}^{'} \left[ \frac{3}{2} + \frac{\sqrt{1+4i_f}+1}{i_f} \right]^{-1} \tag{3.5}$$

where $i_f$ is the normalized forward current [54], given by

$$i_f = ln^2 \left( 1 + exp \left( \frac{V_{GS} - V_T}{2nU_t} \right) \right). \tag{3.6}$$

We substitute (3.6) into (3.5) in order to obtain a $C_{gs}$ equation as a function of gate voltage bias

$$C_{gs_{intrinsic}} = WLC_{ox}^{'} \left[ \frac{3}{2} + \frac{\sqrt{1 + 4ln^2 \left( 1 + exp \left( \frac{V_{GS}-V_T}{2nU_t} \right) \right)} + 1}{ln^2 \left( 1 + exp \left( \frac{V_{GS}-V_T}{2nU_t} \right) \right)} \right]^{-1}. \tag{3.7}$$

The intrinsic capacitance increase happens when channel becomes pinched off at the drain, consequently, the source terminal takes greater control over the channel charge. This can be viewed as, for a given $V_{DS}$, a monotonic increase in source control over the channel charge with $V_{GS}$. So, instead of modeling both forward and reverse currents, we will interpret this as a forward current increase shift regarding to $V_{GS}$. We can implement this delay with respect to $V_{GS}$ in (3.7) by shifting the threshold voltage, we also make the shift proportional to $V_{DS}$. Therefore, (3.7)

becomes

$$C_{gs_{intrinsic}} = WLC'_{ox}\left[\frac{3}{2}+\frac{\sqrt{1+4ln^2\left(1+exp\left(\frac{V_{GS}-V_T+\zeta V_{DS}}{2nU_t}\right)\right)}+1}{ln^2\left(1+exp\left(\frac{V_{GS}-V_T+\zeta V_{DS}}{2nU_t}\right)\right)}\right]^{-1}. \quad (3.8)$$

The intrinsic capacitance increase slope is severely affected by doping profile and short-channel effects [21]. We propose to adjust the ramp up slope of (3.8) by varying the logarithm power in the denominator, leading to

$$C_{gs_{intrinsic}} = WLC'_{ox}\left[\frac{3}{2}+\frac{\sqrt{1+4ln^2\left(1+exp\left(\frac{V_{GS}-V_T+\zeta V_{DS}}{2nU_t}\right)\right)}+1}{ln^{\upsilon}\left(1+exp\left(\frac{V_{GS}-V_T+\zeta V_{DS}}{2nU_t}\right)\right)}\right]^{-1}. \quad (3.9)$$

We assumed extrinsic capacitance to be bias independent. This is justified by good models for extrinsic capacitance which are independent on length as well [34, 35], hence we propose

$$C_{gs_{extrinsic}} = WC'_{gs_{extrinsic}}. \quad (3.10)$$

As stated in Sec. 3.1.1, $C_{gs_{intrinsic}}$ and $C_{gs_{extrinsic}}$ are in parallel [21], therefore we sum both (3.9) and (3.10), leading to

$$C_{gs} = W\left(C'_{gs_{extrinsic}} + LC'_{ox}\left[\frac{3}{2}+\frac{\sqrt{1+4ln^2\left(1+exp\left(\frac{V_{GS}-V_T+\zeta V_{DS}}{2nU_t}\right)\right)}+1}{ln^{\upsilon}\left(1+exp\left(\frac{V_{GS}-V_T+\zeta V_{DS}}{2nU_t}\right)\right)}\right]^{-1}\right) \quad (3.11)$$

where $\zeta$ and $\upsilon$ are obtained through curve fitting.

Short-channel effects are not explicit modeled in (3.11), otherwise, (3.11) would be complex [21]. Hence, the parameters $C'_{gs_{extrinsic}}$ and $C'_{ox}$ will account for short-channel effects if obtained by curve fitting of (3.11). However, if foundry-provided values of $C'_{ox}$ and $C'_{gs_{extrinsic}}$ are used, parameters $\zeta$ and $\upsilon$ will have to handle short-channel effects alone, and (3.11) is still able to fit the $C_{gs}$ behavior with reasonable accuracy as it is demonstrated in Sec. 3.1.3.

In this work, capacitance accuracy is of primary importance. Obtaining $C'_{gs_{extrinsic}}$ is challenging [34], so, we propose to obtain $C'_{gs_{extrinsic}}$ and $C'_{ox}$ by curve fitting, generating a look up table linking the fitted parameters with the transistor sizing and bias. In order to keep the least amount of fitting parameters, we fix $\upsilon$=1, and this proves to be a good value for modeling the process under study. Since $C'_{gs_{extrinsic}}$ and $C'_{ox}$ are obtained through curve fitting, considering short-channel effects, $C'_{gs_{extrinsic}}$ and $C'_{ox}$ might be sensitive to bias. From now on, parameter $\upsilon$ is

replaced by 1 in (3.11), and the $C_{gs}$ model yields

$$C_{gs} = W \left( C'_{gs_{extrinsic}} + LC'_{ox} \left[ \frac{3}{2} + \frac{\sqrt{1 + 4ln^2\left(1 + exp\left(\frac{V_{GS}-V_T+\zeta V_{DS}}{2nU_t}\right)\right) + 1}}{ln\left(1 + exp\left(\frac{V_{GS}-V_T+\zeta V_{DS}}{2nU_t}\right)\right)} \right]^{-1} \right). \tag{3.12}$$

In order to model $C_{gd}$, we take advantage of the saturation assumption mentioned in Sec. 3.1.1. Since the channel becomes pinched-off at the drain in saturation, drain control over the channel charges decreases monotonically with increasing $V_{GS}$. Therefore, we propose to neglect the intrinsic capacitance term in (3.11) for the gate-to-drain capacitance. Hence, we approximate $C_{gd}$ by its extrinsic component

$$C_{gd} = WC'_{gs_{extrinsic}}. \tag{3.13}$$

In this work, we will not advance transistor modeling down to charge distribution levels.

### 3.1.3 Extraction of $C_{gs}$ and $C_{gd}$

The proposed model must hold from sub-threshold to near-threshold operation regions. The $V_{GS}$ upper limit is defined as the gate voltage at which the channel leaves moderate inversion and becomes strongly inverted. A definition for such limit is given by the inversion coefficient which must be equal to 10 [55], and the corresponding $V_{GS}$ for the process under study is 0.75 V. Since $V_{DS}$ and $V_{GS}$ are interchanged depending on which inverter we are interested in, $V_{DS}$ upper limit is also bounded at 750 mV. Once we will be fitting curves using a BSIM model as reference, we avoid setting the lower bound of both $V_{DS}$ and $V_{GS}$ at 0 V due to BSIM problems with $V_{DS}$=0 V [21]. We set $V_{DS}$ and $V_{GS}$ lower limit at 100 mV, because bias dependence is expected to be negligible at such low voltage while still a bit higher than 0 V.

Digital circuits usually use minimum length transistors for compactness and lower capacitances hence, in order to show that the proposed model holds regardless short-channel effects, the model was designed to fit $L$ ranging from 30 nm to 80 nm.

Transistor width has no clear limit for general analog and RF applications, widths about a couple of thousand times bigger than the transistor length can be found nevertheless, as mentioned above, digital applications strive to keep minimum sizes. Hence, we bounded the width from 80 nm to 500 nm, which is enough for our application.

The fitted curves generated, not only in this section, but in this entire chap-

ter, were obtained using the nonlinear least-squares solver from MATLAB. Using the *levenberg-marquardt* algorithm, minimum step toleration of $10^{-30}$ and maximum number of function evaluations of 1000. The minimum search behaves well and converges as long as the initial conditions are close to the results obtained in this thesis. This minimum search is very sensitive to the fitting parameters in the exponents. If the initial conditions are far by no more than one order of magnitude, the minimum search may note converge.

Figs. 3.5, 3.6, 3.7 and 3.8 show $C_{gs}$ for the $n$-type regular $V_T$ and $p$-type low $V_T$ using $L$=30 nm for short-channel effects worst case analysis. The fitted curve using (3.12) is also presented. The fitted parameters can be found in Tabs. 3.1, 3.2, 3.3 and 3.4.

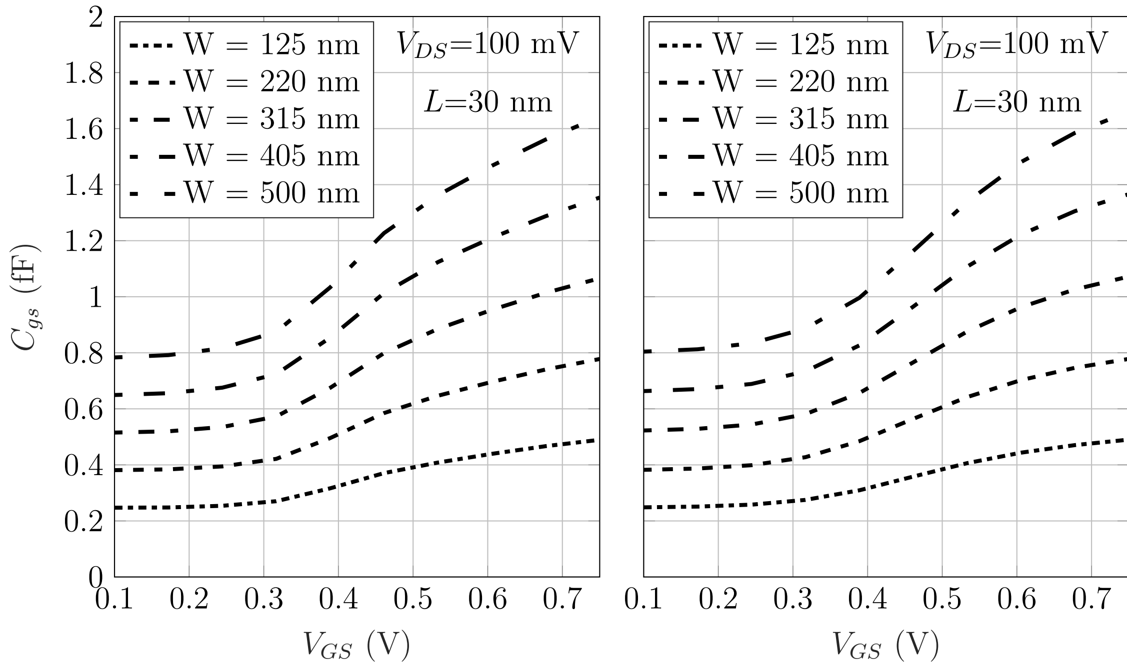


Figure 3.5: $C_{gs}$ obtained from simulations for the $n$-type regular $V_T$ (left) and their corresponding fitted curves using (3.12) (right) for $V_{DS}$=100 mV and $L$=30 nm.

Table 3.1: Fitted parameters of (3.12) used in Fig. 3.5.

| $W$ (nm) | $C'_{gs_{extrinsic}}$ (aF/nm) | $C'_{ox}$ (zF/nm$^2$) | $\zeta$ |
|---|---|---|---|
| 125 | 1.9487 | 92.259 | 0.1409 |
| 220 | 1.7253 | 87.208 | 0.3058 |
| 315 | 1.6571 | 85.648 | 0.2994 |
| 405 | 1.6208 | 84.941 | 0.2798 |
| 500 | 1.5987 | 84.516 | 0.2644 |

Figs. 3.5, 3.6, 3.7 and 3.8 show that both simulations and (3.12) are in close agreement in fact, the maximum and mean errors are smaller than 5.2% as observed

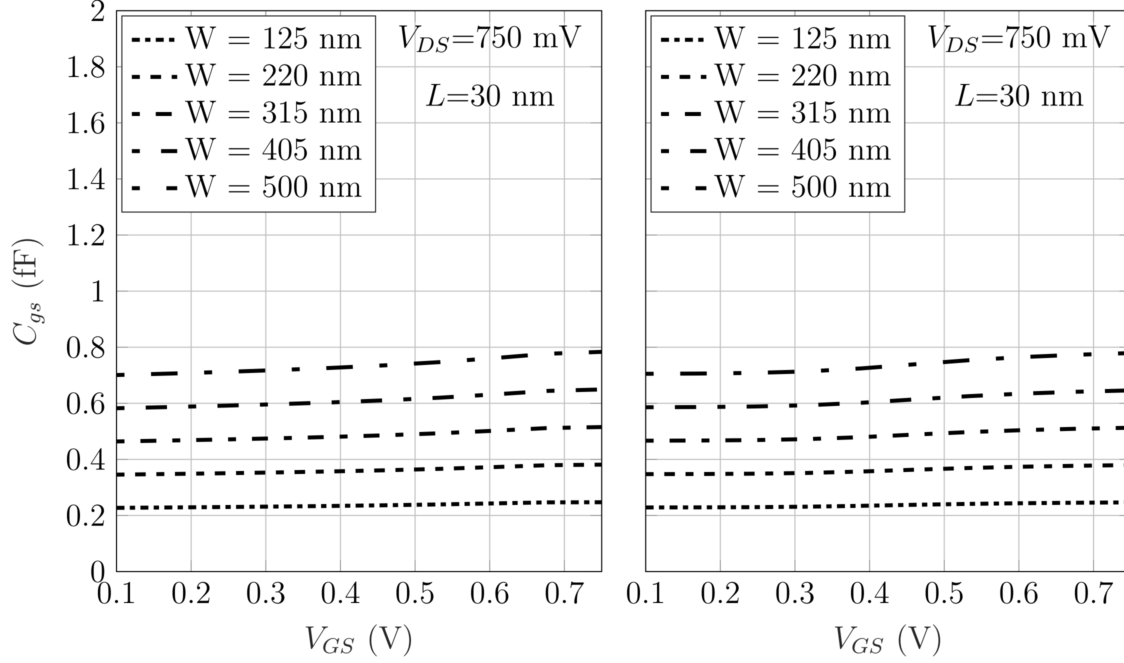


Figure 3.6: $C_{gs}$ obtained from simulations for the $n$-type regular $V_T$ (left) and their corresponding fitted curves using (3.12) (right) for $V_{DS}$=750 mV and $L$=30 nm.

Table 3.2: Fitted parameters of (3.12) used in Fig. 3.6.

| $W$ (nm) | $C'_{gs_{extrinsic}}$ (aF/nm) | $C'_{ox}$ (zF/nm$^2$) | $\zeta$ |
|---|---|---|---|
| 125 | 1.8025 | 6.743 | 0.0589 |
| 220 | 1.5777 | 7.036 | 0.0582 |
| 315 | 1.4883 | 7.113 | 0.0580 |
| 405 | 1.4399 | 7.157 | 0.0578 |
| 500 | 1.4097 | 7.186 | 0.0578 |

Table 3.3: Fitted parameters of (3.12) used in Fig. 3.7.

| $W$ (nm) | $C'_{gs_{extrinsic}}$ (aF/nm) | $C'_{ox}$ (zF/nm$^2$) | $\zeta$ |
|---|---|---|---|
| 125 | 1.7697 | 5.534 | 0.1031 |
| 220 | 1.5967 | 5.387 | 0.1225 |
| 315 | 1.5257 | 5.458 | 0.1320 |
| 405 | 1.4872 | 5.517 | 0.1377 |
| 500 | 1.4630 | 5.560 | 0.1414 |

in Tab. 3.5 however, good accuracy can be reached for different functions if enough parameters are used even if the provided functions have no physical background.

Accuracy is necessary but, we want that each parameter in the proposed equation inherits the physical meaning of its parent equations ((3.5), (3.6) and (3.10)). The fitted parameters $C'_{gs_{extrinsic}}$ and $C'_{ox}$ are expected to be independent of width, length and bias (not considering second order effects such as hot carrier oxide degradation

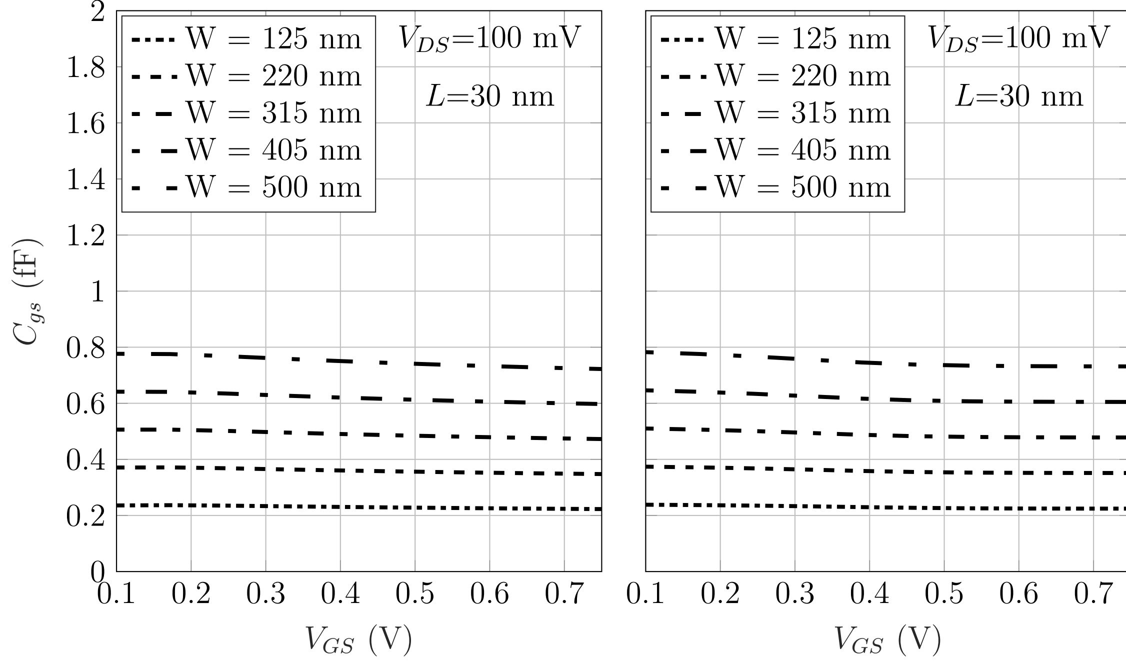


Figure 3.7: $C_{gs}$ obtained from simulations for the $p$-type low $V_T$ (left) and their corresponding fitted curves using (3.12) (right) for $V_{DS}$=100 mV and $L$=30 nm.

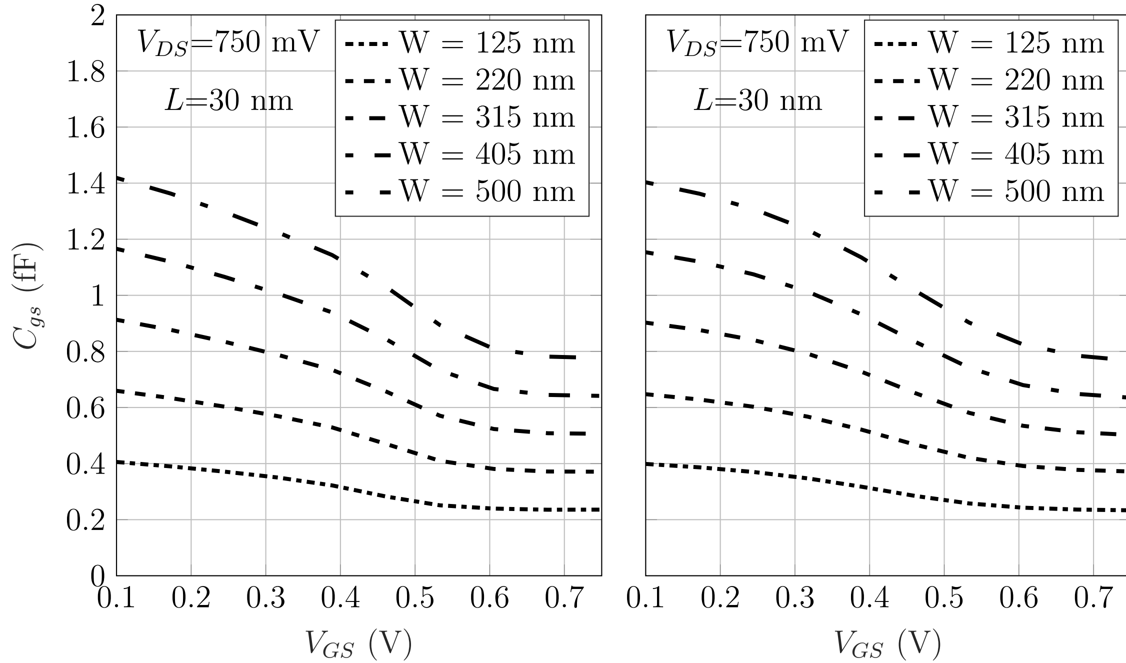


Figure 3.8: $C_{gs}$ obtained from simulations for the $p$-type low $V_T$ (left) and their corresponding fitted curves using (3.12) (right) for $V_{DS}$=750 mV and $L$=30 nm.

[21, 34]) therefore, they should remain approximately constant for the simulations presented in Figs. 3.5, 3.6, 3.7 and 3.8. On the other hand, parameter $\zeta$ models short-channel effects by shifting the threshold voltage therefore, it is expected to be a strong function of length and, maybe, width if the channel is too narrow.

Table 3.4: Fitted parameters of (3.12) used in Fig. 3.8.

| $W$ (nm) | $C'_{gs_{extrinsic}}$ (aF/nm) | $C'_{ox}$ (zF/nm$^2$) | $\zeta$ |
|---|---|---|---|
| 125 | 1.8275 | 62.744 | -0.0527 |
| 220 | 1.6727 | 60.084 | -0.1097 |
| 315 | 1.5815 | 61.128 | -0.1401 |
| 405 | 1.5384 | 60.984 | -0.1556 |
| 500 | 1.5106 | 60.775 | -0.1654 |

Table 3.5: Mean and maximum error between simulations and fitted curves presented in Figs. 3.5, 3.6, 3.7 and 3.8.

| $V_{DS}$=100 mV | | | | |
|---|---|---|---|---|
| $W$ (nm) | $n$-type mean (%) | $n$-type max (%) | $p$-type mean (%) | $p$-type max (%) |
| 125 | 1.3 | 3.4 | 0.4 | 1.1 |
| 220 | 1.2 | 3.5 | 0.5 | 1.1 |
| 315 | 1.7 | 4.1 | 0.5 | 1.2 |
| 405 | 2.0 | 4.8 | 0.5 | 1.3 |
| 500 | 2.3 | 5.2 | 0.6 | 1.3 |
| $V_{DS}$=750 mV | | | | |
| $W$ (nm) | $n$-type mean (%) | $n$-type max (%) | $p$-type mean (%) | $p$-type max (%) |
| 125 | 0.4 | 0.8 | 1.1 | 2.7 |
| 220 | 0.4 | 0.8 | 1.6 | 3.3 |
| 315 | 0.5 | 0.9 | 1.0 | 2.2 |
| 405 | 0.5 | 0.9 | 1.0 | 2.1 |
| 500 | 0.5 | 0.9 | 0.9 | 1.9 |

Analyzing the parameters in Tabs. 3.1 and 3.2, we note that $C'_{gs_{extrinsic}}$ and $C'_{ox}$ remain nearly constant for different transistor widths nevertheless, $C'_{ox}$ changes an order of magnitude if we switch $V_{DS}$ from 100 mV to 750 mV, which is conflicting with the $C'_{ox}$ definition. This can be explained by two reasons: first, $C'_{ox}$ should not be obtained through curve fitting, because $C'_{ox}$ and short-channel effects cannot be distinguished in the intrinsic capacitance component in (3.12). Second, (3.12) is not expected to provide constant $C'_{gs_{extrinsic}}$ and $C'_{ox}$ due to the simplification from (3.11) where we fixed $\upsilon$=1.

Extensive simulations and validation of (3.11) will not be provided, but we will advocate (3.11). Since we believe its compactness, physical background and potential to predict $C_{gs}$ including short-channel effects might be a contribution, we illustrate that (3.11) has the potential to hold the aforementioned features with one curve fitting.

Fig. 3.9 is an example of curve fitting for $V_{DS}$=750 mV using (3.11) where $\upsilon$ of (3.9) is now a fitting parameter, and $C'_{ox}$ and $C'_{gs_{extrinsic}}$ are the same from the fitted

curve using $V_{DS}$=100 mV (Fig. 3.5).

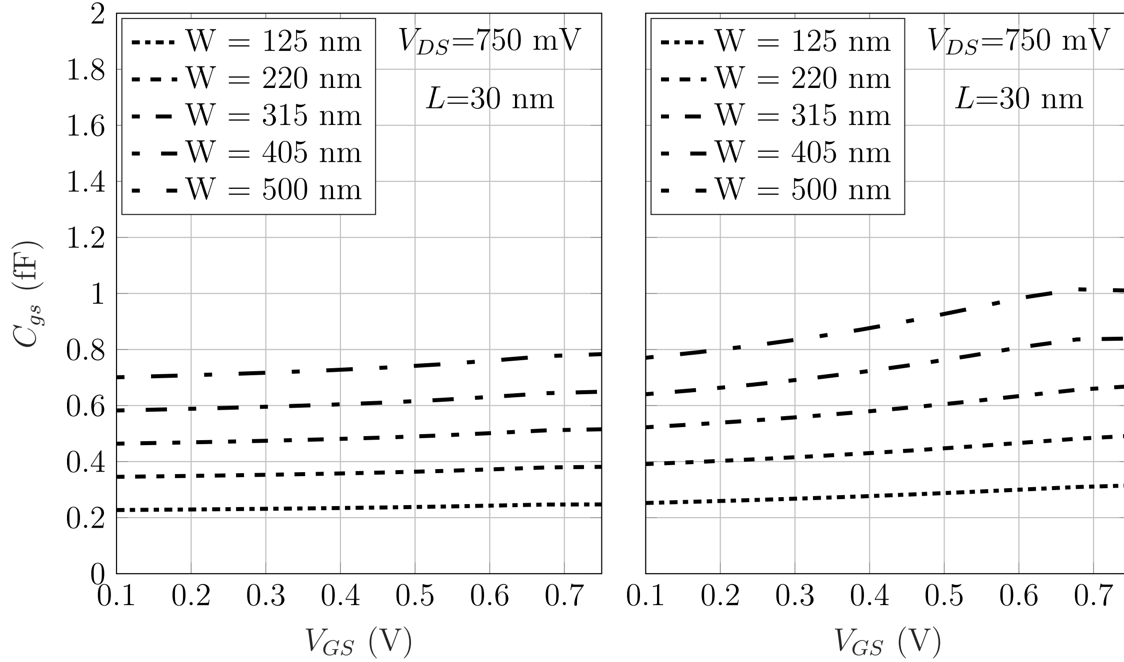


Figure 3.9: $C_{gs}$ obtained from simulations for the $n$-type regular $V_T$ (left) and their corresponding fitted curves using (3.11) (right) for $V_{DS}$=750 mV and $L$=30 nm.

Table 3.6: Fitted parameters of (3.11) used in Fig. 3.9.

| $W$ (nm) | $\zeta$ | $\upsilon$ |
|---|---|---|
| 125 | -0.4931 | 0.1014 |
| 220 | -0.4906 | 0.0981 |
| 315 | -0.4606 | 0.1079 |
| 405 | -0.3844 | 0.1342 |
| 500 | -0.3562 | 0.1406 |

The fitted curves in Fig. 3.9 had mean error lower than 9% and maximum error lower than 17%, which shows that, even with only two fitting parameters, (3.11) has enough degrees of freedom to grasp the $C_{gs}$ behavior however, a better model for $\zeta$ and $\upsilon$ should be advanced, in view of the fact that parameters $\zeta$ and $\upsilon$ showed to be dependent on transistor dimensions and bias.

Simulations in Figs. 3.10, 3.11, 3.12 and 3.13 were carried out for $L$=80 nm in order to verify that (3.12) holds if short-channel effects are reduced. The fitted parameters used in (3.12) can be found in Tabs. 3.7, 3.8, 3.9 and 3.10. Mean and maximum errors between simulation and the fitted curves in Figs. 3.10, 3.11, 3.12 and 3.13 can be observed in Tab. 3.11. The fitted curves are in close agreement with simulations for most of the design region, showing that obtaining the parameters of (3.12) by a look up table can provide good accuracy.

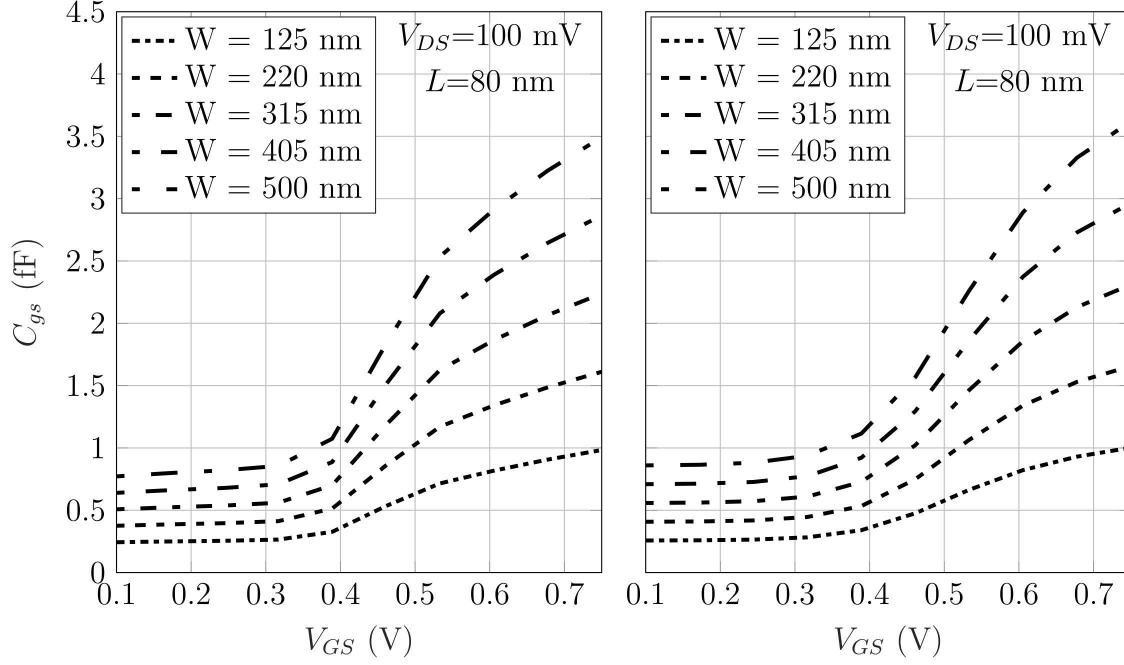


Figure 3.10: $C_{gs}$ obtained from simulations for the $n$-type regular $V_T$ (left) and the corresponding fitted curves using (3.12) (right) for $V_{DS}$=100 mV and $L$=80 nm.

Table 3.7: Fitted parameters of (3.12) used in Fig. 3.10.

| $W$ (nm) | $C'_{gs_{extrinsic}}$ (aF/nm) | $C'_{ox}$ (zF/nm$^2$) | $\zeta$ |
|---|---|---|---|
| 125 | 2.0261 | 105.146 | 0.0414 |
| 220 | 1.8486 | 102.431 | 0.0424 |
| 315 | 1.7781 | 101.356 | 0.0424 |
| 405 | 1.7402 | 100.784 | 0.0423 |
| 500 | 1.7166 | 100.429 | 0.0422 |

Table 3.8: Fitted parameters of (3.12) used in Fig. 3.11.

| $W$ (nm) | $C'_{gs_{extrinsic}}$ (aF/nm) | $C'_{ox}$ (zF/nm$^2$) | $\zeta$ |
|---|---|---|---|
| 125 | 1.7655 | 2.336 | 0.0096 |
| 220 | 1.5450 | 2.422 | 0.0096 |
| 315 | 1.4563 | 2.455 | 0.0096 |
| 405 | 1.4083 | 2.475 | 0.0096 |
| 500 | 1.3782 | 2.487 | 0.0096 |

Table 3.9: Fitted parameters of (3.12) used in Fig. 3.12.

| $W$ (nm) | $C'_{gs_{extrinsic}}$ (aF/nm) | $C'_{ox}$ (zF/nm$^2$) | $\zeta$ |
|---|---|---|---|
| 125 | 1.7451 | 1.663 | 0.0117 |
| 220 | 1.5726 | 1.654 | 0.0125 |
| 315 | 1.5027 | 1.655 | 0.0128 |
| 405 | 1.4638 | 1.652 | 0.0130 |
| 500 | 1.4401 | 1.654 | 0.0131 |

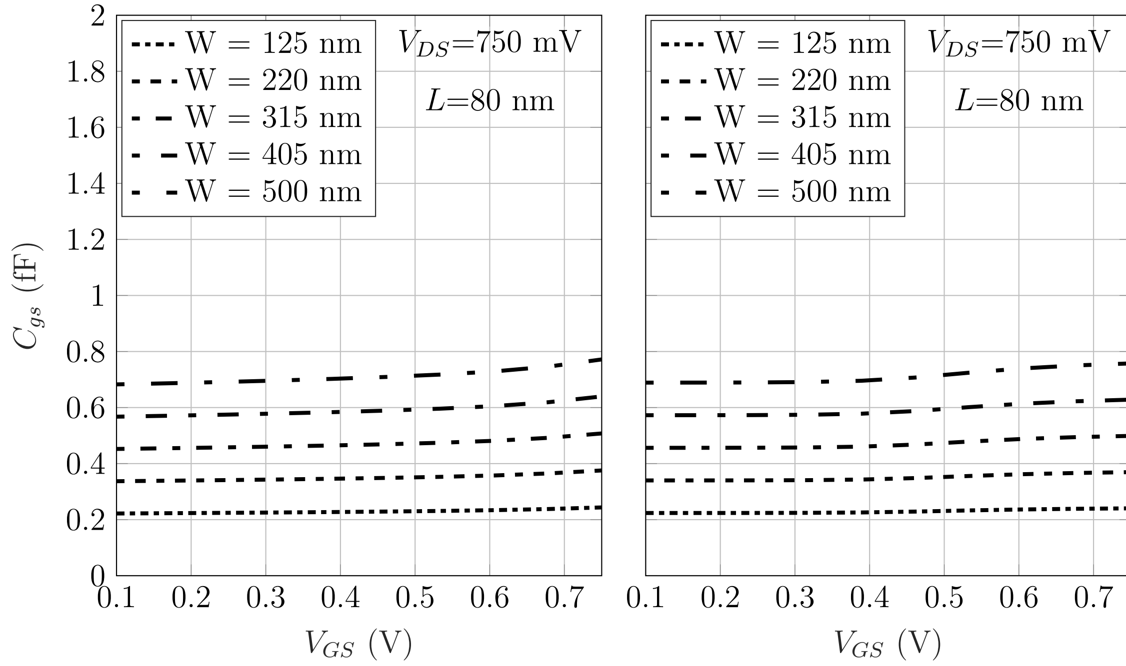


Figure 3.11: $C_{gs}$ obtained from simulations for the $n$-type regular $V_T$ (left) and the corresponding fitted curves using (3.12) (right) for $V_{DS}$=750 mV and $L$=80 nm.

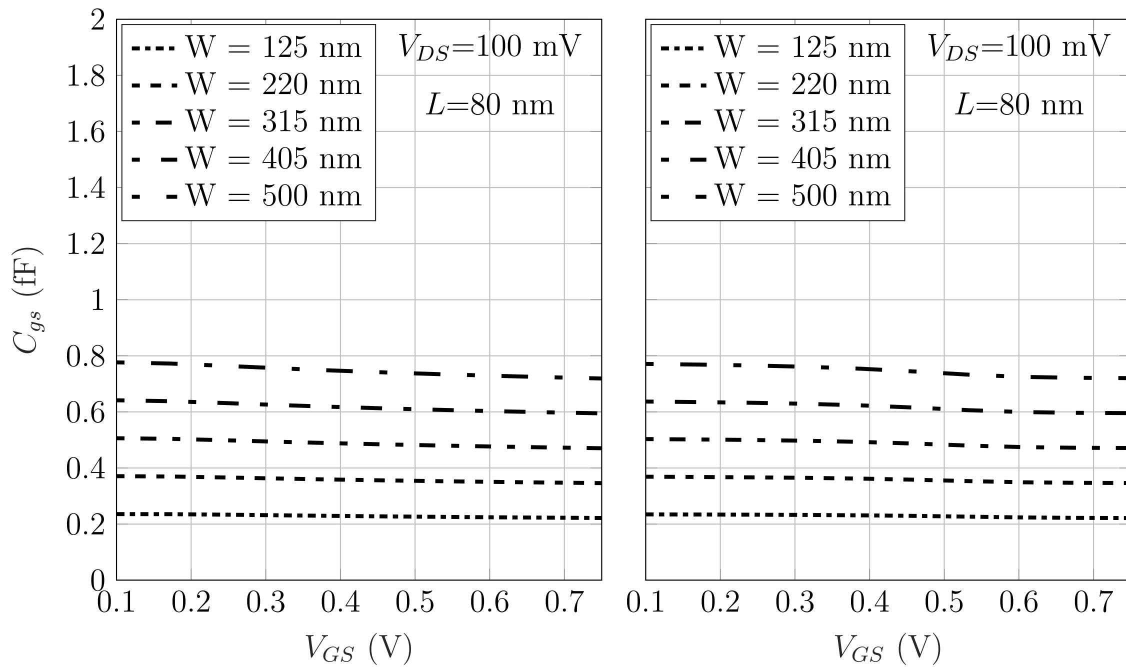


Figure 3.12: $C_{gs}$ obtained from simulations for the $p$-type low $V_T$ (left) and the the corresponding fitted curve using (3.12) (right) for $V_{DS}$=100 mV and $L$=80 nm.

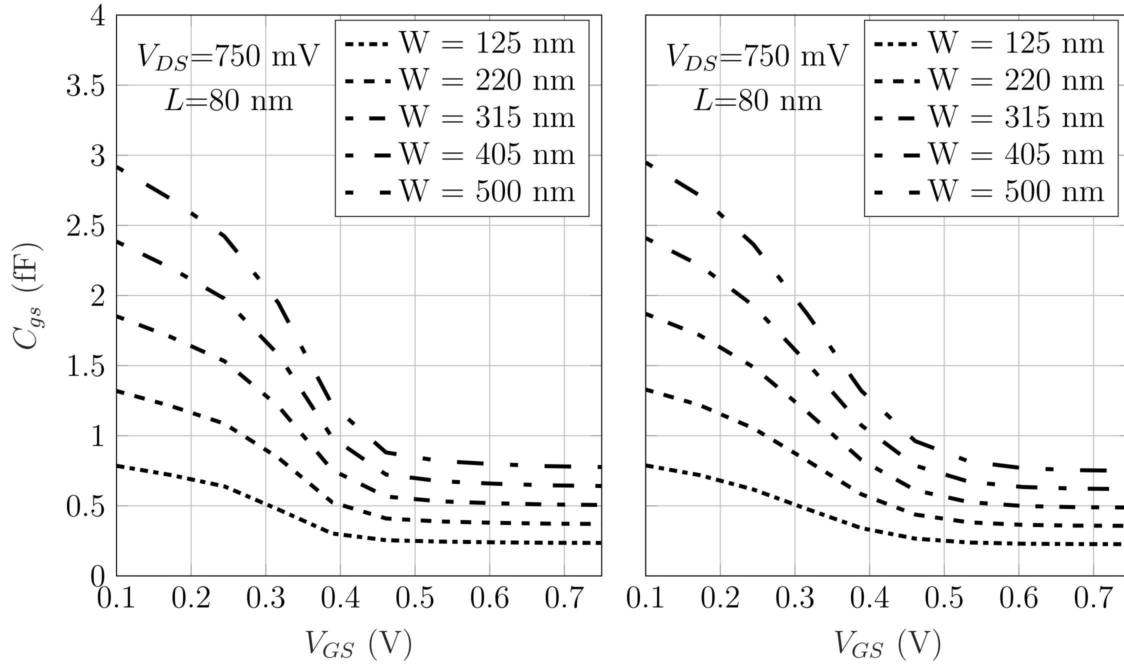


Figure 3.13: $C_{gs}$ obtained from simulations for the $p$-type low $V_T$ (left) and the the corresponding fitted curve using (3.12) (right) for $V_{DS}$=750 mV and $L$=80 nm.

| $W$ (nm) | $C'_{gs_{extrinsic}}$ (aF/nm) | $C'_{ox}$ (zF/nm$^2$) | $\zeta$ |
|---|---|---|---|
| 125 | 1.7840 | 83.244 | 0.2968 |
| 220 | 1.6203 | 81.950 | 0.2474 |
| 315 | 1.5537 | 81.298 | 0.2250 |
| 405 | 1.5197 | 80.906 | 0.2122 |
| 500 | 1.4964 | 80.641 | 0.2039 |

Table 3.10: Fitted parameters of (3.12) used in Fig. 3.13.

Table 3.11: Mean and maximum error between simulations and fitted curves presented in Figs. 3.10, 3.12, 3.11 and 3.13.

| $V_{DS}$=100 mV | | | | |
|---|---|---|---|---|
| $W$ (nm) | $n$-type mean (%) | $n$-type max (%) | $p$-type mean (%) | $p$-type max (%) |
| 125 | 4.7 | 10.9 | 0.4 | 0.8 |
| 220 | 6.0 | 12.9 | 0.4 | 0.9 |
| 315 | 6.7 | 13.8 | 0.4 | 0.9 |
| 405 | 7.1 | 14.3 | 0.4 | 0.8 |
| 500 | 7.4 | 14.7 | 0.5 | 0.8 |
| $V_{DS}$=750 mV | | | | |
| $W$ (nm) | $n$-type mean (%) | $n$-type max (%) | $p$-type mean (%) | $p$-type max (%) |
| 125 | 0.6 | 1.3 | 11.1 | 31.4 |
| 220 | 0.7 | 1.6 | 7.5 | 21.2 |
| 315 | 0.8 | 1.7 | 6.1 | 17.2 |
| 405 | 0.8 | 1.8 | 5.6 | 15.1 |
| 500 | 0.8 | 1.8 | 5.3 | 13.8 |

### 3.1.4 $C_{gb}$ Model

Gate-to-bulk capacitance can also be decomposed into extrinsic and intrinsic capacitances [21]. The extrinsic part is related to the capacitive coupling between the gate and bulk plates, which is approximately bias independent. Since the bulk and gate terminals do modulate depletion and inversion charges, a intrinsic component takes place as well. In the following analysis, we will first assume that $C_{gb}$ is bias independent.

In Fig. 3.14 the $C_{gb}$ behavior by varying transistor width and length can be observed, both drain and gate bias voltages are fixed at 100 mV. From this simulation, we can observe that, if everything but bias voltages are constant, both $L$ and $W$ have a linear relationship with $C_{gb}$. However, the slope of $C_{gb}(W)$ increases for different values of $L$ similarly, the slope $C_{gb}(L)$ also increases with increasing $W$. The classical area/perimeter equation can model such behavior therefore, $C_{gb}$ is given by

$$C_{gb} = C'_{gb_A} WL + C'_{gb_W} W + C'_{gb_L} L \tag{3.14}$$

where $C'_{gb_A}$ is the fitted gate-to-bulk capacitance per area, $C'_{gb_W}$ is the fitted gate to bulk capacitance per transistor width and $C'_{gb_L}$ is the fitted gate-to-bulk capacitance per transistor length.

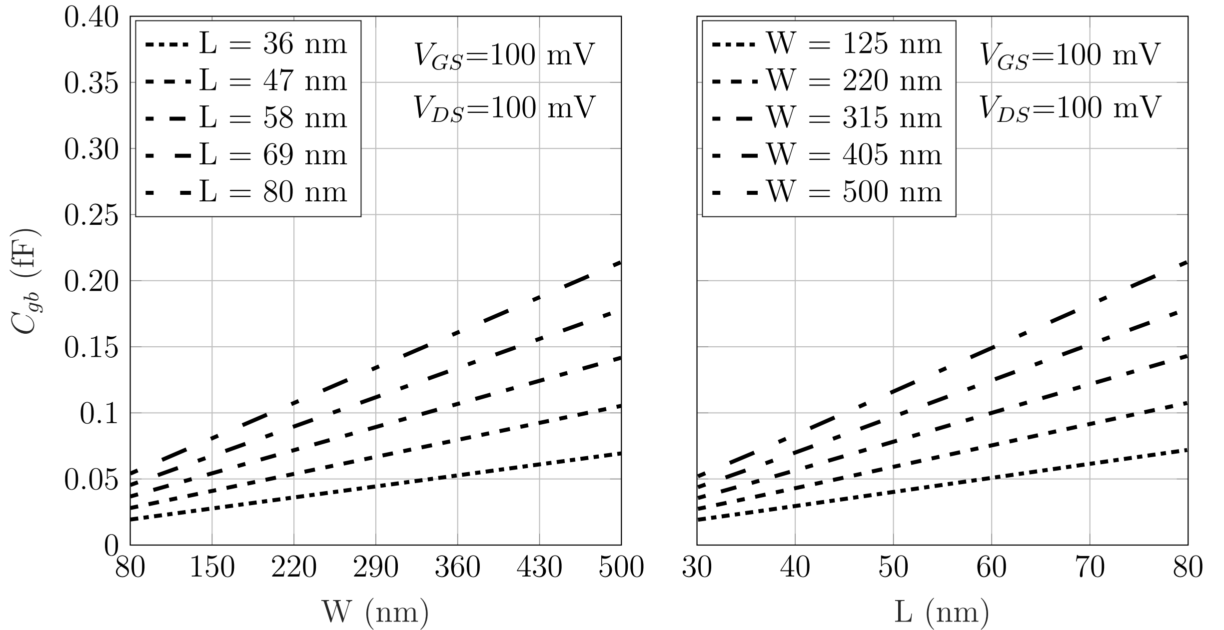


Figure 3.14: Simulated $n$-type regular $V_T$ gate-to-bulk capacitance behavior as a function of transistor width for different values of $L$ (left) and as a function of transistor length for different values of $W$ (right).

Bias effects on $C_{gb}$ can be observed in Fig. 3.15. Simulations were carried out for the width and length corners of the region defined in Sec. 3.1.3. For the design region

corner with $L$=80 nm and $W$=500 nm, $C_{gb}$ had the highest sensitivity, 4.827 aF/V for $C_{gb}(V_{GS})$ and 6.623 aF/V for $C_{gb}(V_{DS})$). Since the sensitivity of $C_{gb}$ with $W$ and $L$ is significantly higher than with bias, approximating $C_{gb}$ to be bias independent justifies the model given by (3.14).

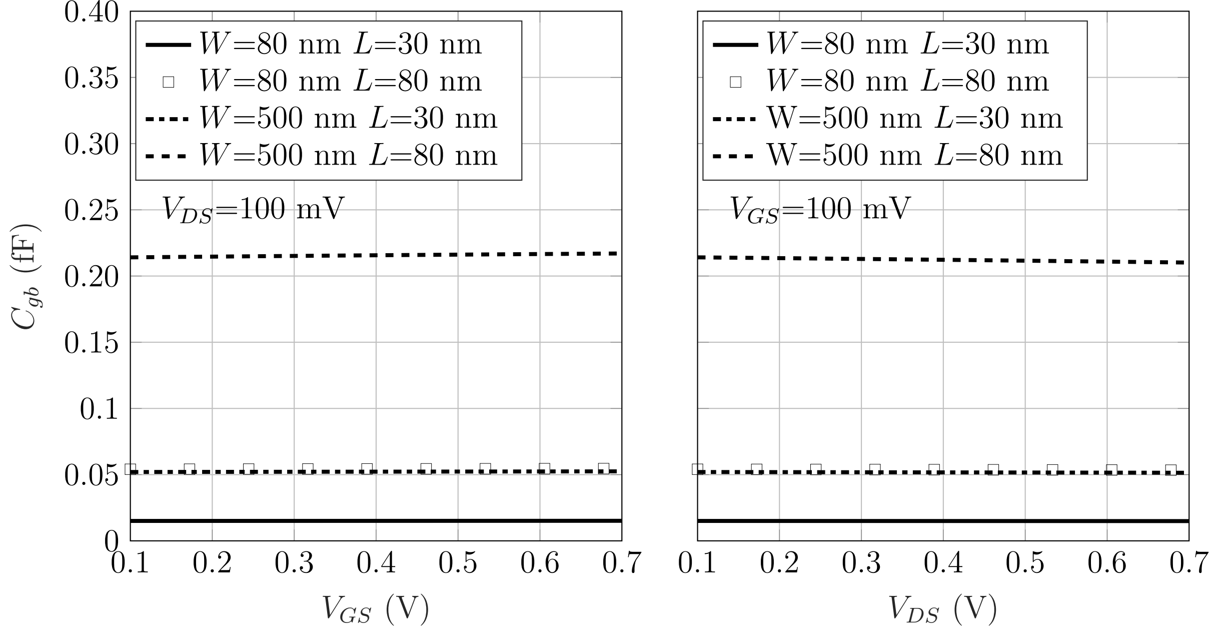


Figure 3.15: Simulated $n$-type regular $V_T$ gate-to-body capacitance behavior as a function of $V_{GS}$ (left) and as a function of $V_{DS}$ (right).

### 3.1.5 Extraction of $C_{gb}$

The extraction of $C_{gb}$ will be carried out for the same design region defined in Sec. 3.1.3. In Figs. 3.16 and 3.17 can be found the simulated $C_{gb}$ and the fitted curves using (3.14) for both $p$ and $n$-type transistors. Although bias effects are negligible, in order to minimize capacitance errors due to bias, we fitted $C_{gb}$ close to the middle of the bias range ($V_{GS}$=390 mV and $V_{DS}$=390 mV). The fitted parameters can be found in Tab. 3.12. Mean and maximum errors are presented in Tab. 3.13.

Table 3.12: Fitted parameters of (3.14) used in Figs. 3.16 and 3.17.

| $n$-type | $C'_{gb_A}$ (aF/nm$^2$) | $C'_{gb_W}$ (yF/nm) | $C'_{gb_L}$ (yF/nm) |
|---|---|---|---|
| | 0.59723 | -0.0950 | 0.2904 |

| $p$-type | $C'_{gb_A}$ (aF/nm$^2$) | $C'_{gb_W}$ (yF/nm) | $C'_{gb_L}$ (yF/nm) |
|---|---|---|---|
| | 0.54585 | -0.1006 | 0.3196 |

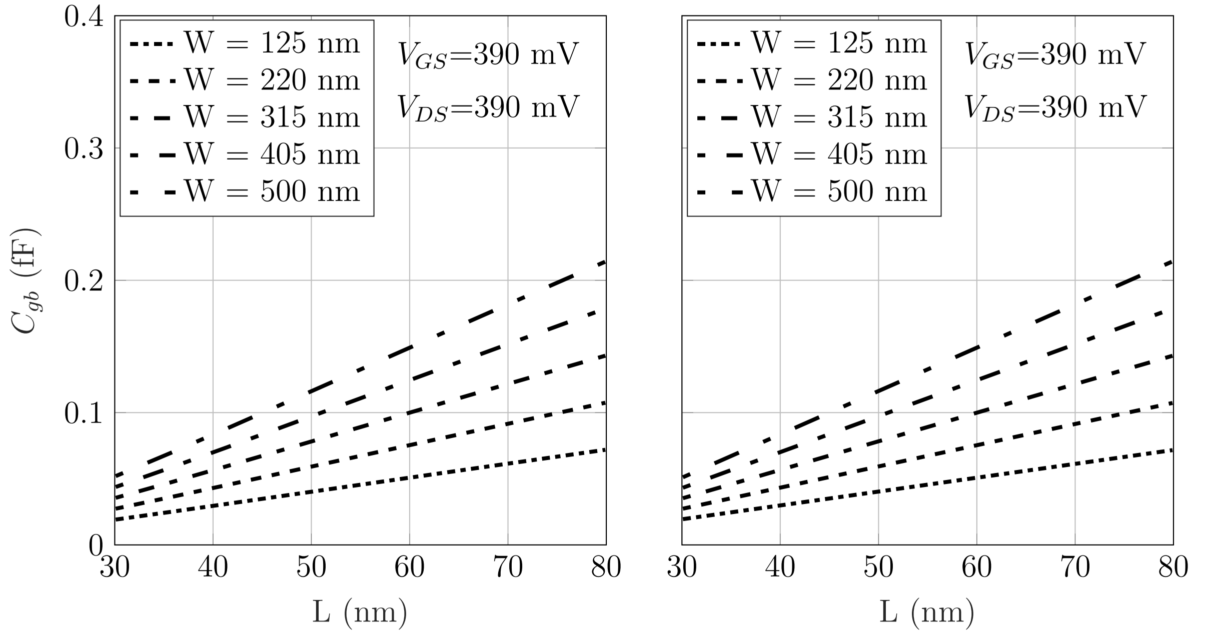


Figure 3.16: Simulated $n$-type regular $V_T$ gate-to-body capacitance behavior as a function of transistor width for different values of $L$ (left) and the fitted curve using (3.14) (right).

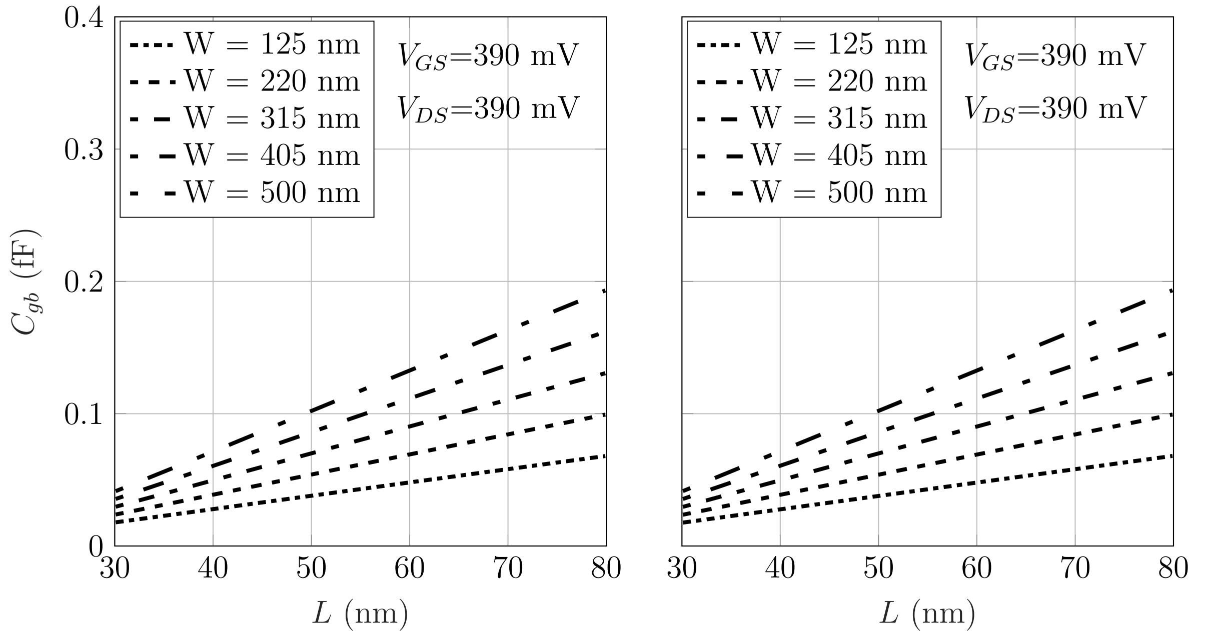


Figure 3.17: Simulated $p$-type low $V_T$ gate-to-body capacitance behavior as a function of transistor width for different values of $L$ (left) and the fitted curve using (3.14) (right).

Figs 3.16 and 3.17 show the close agreement between simulation and the fitted curves. It is also confirmed by the obtained errors in Tab. 3.13. Although $C_{gb}$ was approximated to be bias independent, using the fitted parameter of Tab. 3.12 in (3.14) still provides very accurate capacitance values for any bias inside the design

Table 3.13: Mean and maximum error between simulations and fitted curves presented in Figs. 3.16 and 3.17.

| $W$ (nm) | $n$-type mean (%) | $n$-type max (%) | $p$-type mean (%) | $p$-type max (%) |
|---|---|---|---|---|
| 125 | 0.6 | 1.7 | 0.4 | 1.2 |
| 220 | 0.2 | 0.7 | 0.2 | 0.7 |
| 315 | 0.2 | 0.8 | 0.1 | 0.4 |
| 405 | 0.2 | 1.3 | 0.1 | 0.3 |
| 500 | 0.2 | 1.7 | 0.1 | 0.4 |

region with maximum error below 2.7% for the $n$-type and below 1.5% for the $p$-type.

### 3.1.6 $C_j$ Model

The capacitance formed by the source/drain region with bulk is called junction capacitance. Since inversion region and depletion charges are correlated, the depletion between source/drain and bulk does behave somewhat different comparing with the classical reversed bias $pn$ junction capacitance which does not invert. As mentioned, because inversion and depletion charges are correlated, $C_j$ must have an intrinsic component nonetheless, it is notably small for the process under study for two reasons: first, source is connected to the bulk, hence reducing body effect which enhances junction capacitance, second, the circuit is designed to work with very limited supply voltages, therefore, depletion and inversion charges are less present than for operations above threshold.

In Fig. 3.18 is presented the $n$-type regular $V_T$ junction capacitance variation with both $V_{GS}$ and $V_{DS}$ for different transistor sizes. The highest sensitivity with bias can be observed for the simulations with the largest transistor dimensions inside the design region, which is given by 0.7731 aF/V by varying $V_{GS}$ and roughly 0 for $V_{DS}$, justifying the bias independence approximation.

Transistor length is also known to not influence $C_j$ because it does not affect the source/drain region geometry, however, due to charge sharing effects, source and drain might communicate with each other if the channel is very short. Deeper insight on short channel effects in $C_j$ behavior can be observed in Fig. 3.19. Note that the simulation for $L$=30 nm had the highest deviation among the curves in fact, $C_{gb}$ becomes less sensitive to transistor length as $L$ increases (Fig. 3.20).

Finally, we study the $C_j$ behavior with $W$. Junction capacitance is related to the geometry of the source and drain regions, i.e. diffusion length, width and depth. Designers do not have control over all the parameters mentioned unless they design a bipolar circuit [56]. Since this work is focused in digital applications, very stringent rules and best practices must be followed, which takes diffusion length and deepness

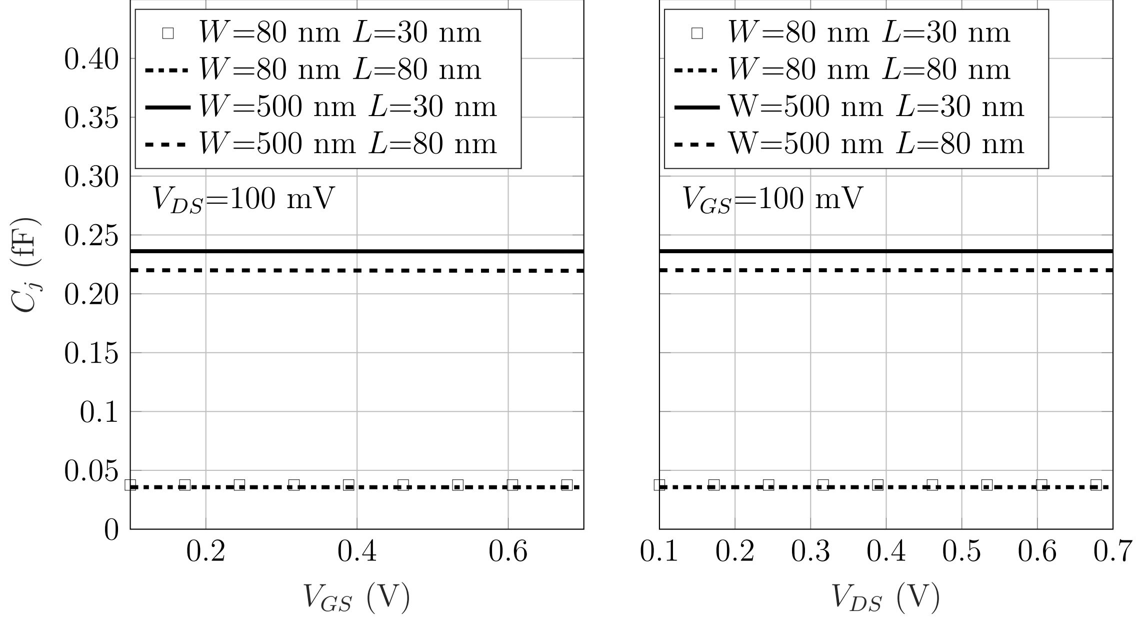


Figure 3.18: $C_j$ behavior of the $n$-type regular $V_T$ for different values of $W$ and $L$ as a function of $V_{GS}$ (left) and as a function of $V_{DS}$ (right).

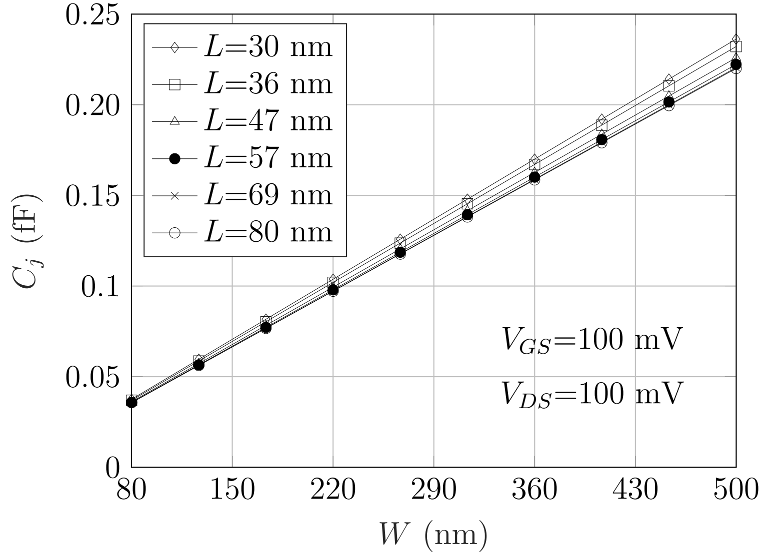


Figure 3.19: $C_j$ behavior of the $n$-type regular $V_T$ as a function of $W$ varying $L$ for fixed $V_{DS}$ and $V_{GS}$.

out of the designer control.

The diffusion width is the same as the transistor width, because both sides of the channel and source/drain belongs to the same wall. Therefore, the capacitance is proportional to $W$. Such behavior can be observed in Fig. 3.19.

Since transistor length has little effect of junction capacitance (16 aF for transistor length ranging from 30 nm to 80 nm as observed in Fig. 3.20), we propose to approximate $C_j$ to be independent on transistor length, leaving junction capacitance as a function of $W$ only. Noting that the $C_j$ clearly has a linear relationship with

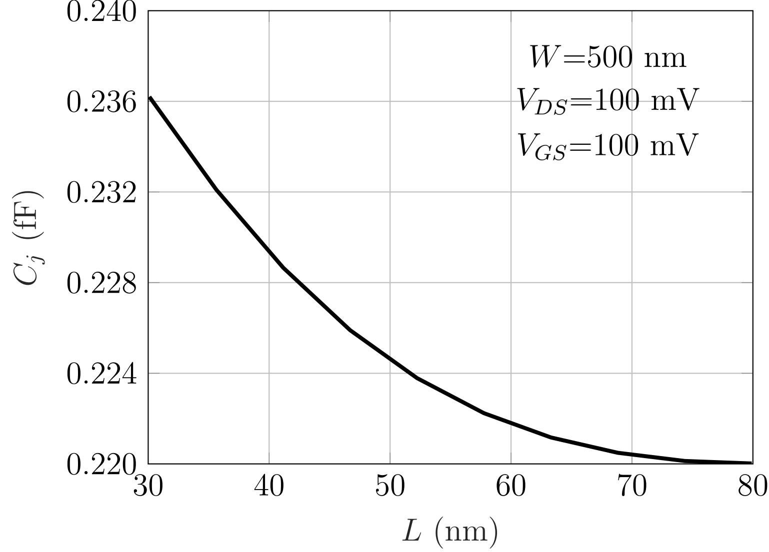


Figure 3.20: Simulated $n$-type $C_j$ varying transistor length and fixed width and bias voltages.

$W$ inside the simulated region, we propose

$$C_j = C'_{jw} W \tag{3.15}$$

where $C'_{jw}$ is the fitted junction capacitance density per transistor width.

### 3.1.7 Extraction of $C_j$

The design region covered by bias and transistor sizing remains the same as in the previous sections. Simulated and fitted curves using (3.15) can be observed in Figs. 3.21 and 3.22. Both $V_{GS}$ and $V_{DS}$ were fixed at 390 mV in order to minimize mean and maximum errors between model and simulation across the bias range. $L$ was fixed at 80 nm in order to minimize short channel effects. The fitted parameters and mean and maximum errors are presented in Tabs. 3.14 and 3.15, respectively.

Table 3.14: Fitted parameters of (3.15) to be used in Figs. 3.21 and 3.22.

| $n$-type | $C'_{jw}$ (aF/nm) | $p$-type | $C'_{jw}$ (aF/nm) |
|---|---|---|---|
| | 0.4401 | | 0.4502 |

Table 3.15: Mean and maximum error between simulations and fitted curves presented in Figs. 3.21 and 3.22.

| $n$-type mean (%) | $n$-type max (%) | $p$-type mean (%) | $p$-type max (%) |
|---|---|---|---|
| 0.3 | 1.2 | 0.2 | 0.7 |

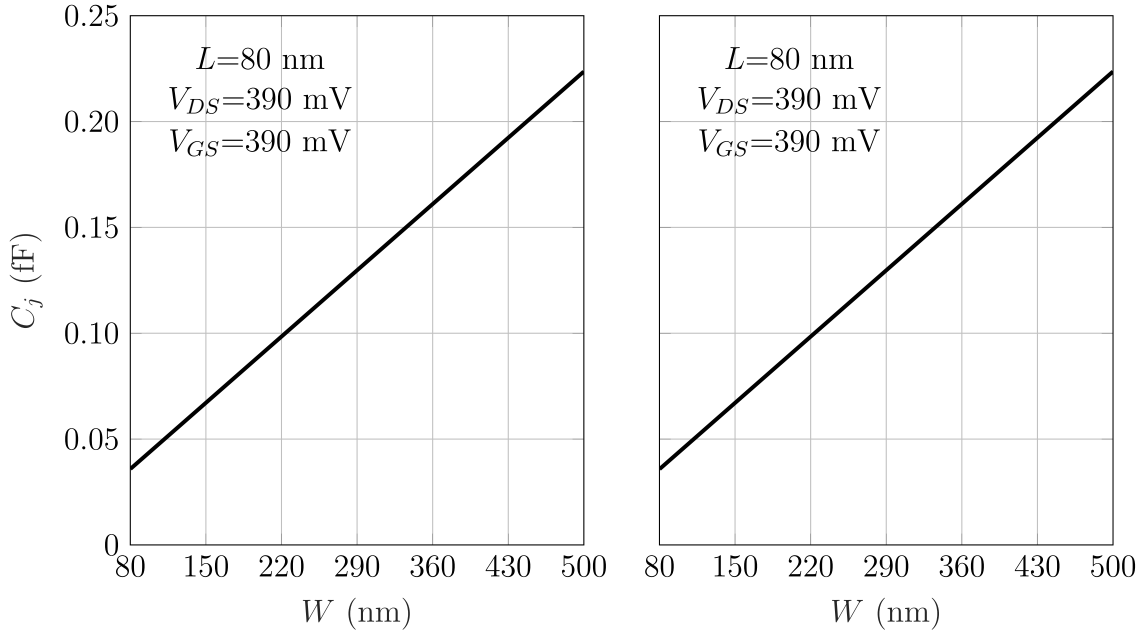


Figure 3.21: Simulated $n$-type regular $V_T$ junction capacitance behavior as a function of transistor width for fixed values of $L$ and bias (left) and the fitted curve using (3.15) (right).

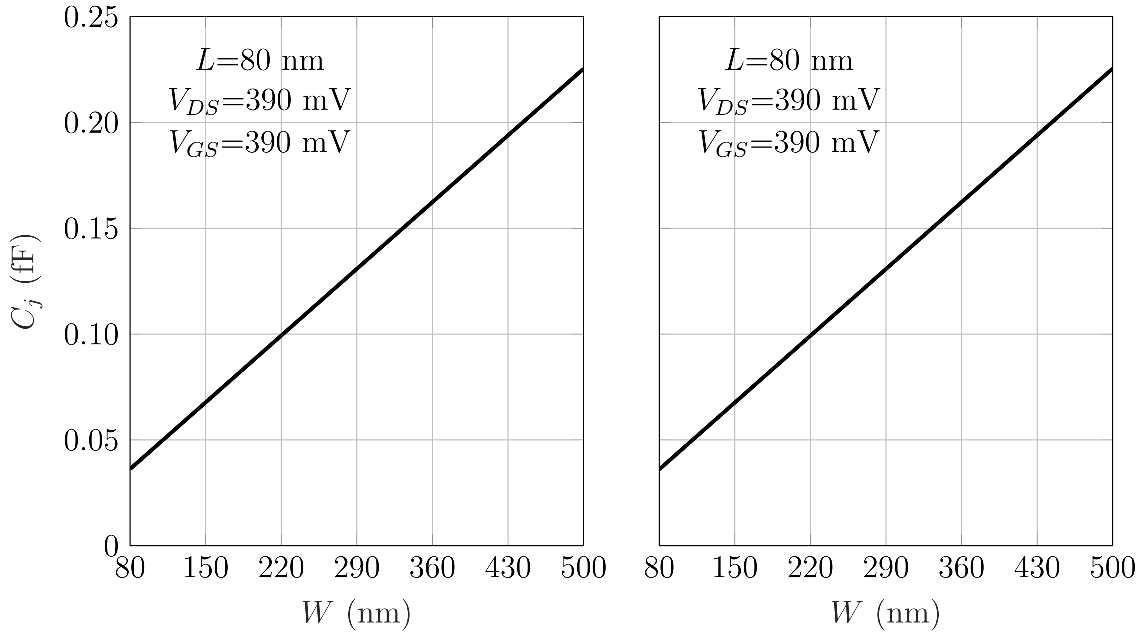


Figure 3.22: Simulated $p$-type low $V_T$ junction capacitance behavior as a function of transistor width for fixed values of $L$ and bias (left) and the fitted curve using (3.15) (right).

Observation of Figs. 3.21 and 3.22 suggests that both simulations and (3.15) are in close agreement, Tab. 3.15 confirms it. As mentioned, $C_j$ sensitivity on $V_{GS}$ and $V_{DS}$ is extremely low. In fact, $n$-type maximum error worst case is 1.3 % for $V_{GS}$=100 mV for the $p$-type, the maximum error is 0.7 % with $V_{GS}$=750 mV. Junction capacitance

showed to be insensitive to $V_{DS}$.

Among the simplifications, the most important is to neglect the transistor length. As observed in Fig. 3.20, the capacitance for the $n$-type varies 16 aF for $L$ ranging from 30 nm to 80 nm. This represents a maximum error of 6.8 %. For the $p$-type, $C_j$ changes only 5 aF for $L$ ranging from 30 nm to 80 nm, this leads to a maximum error of 2.0 %.

## 3.2 Transconductance

In this section we present a compact MOSFET transconductance equation which has been derived from the EKV model. The need of a simple equation for transconductance which holds through weak to strong inversion is of special interest for IoT applications, because supply voltages are very limited [57] and the speed-power product optimum usually resides in near-threshold supplies voltages [16, 17]. The transconductance model presented in this work not only holds for weak and moderate inversion but is still fairly accurate in strong inversion as well. Furthermore, the model is simple and useful for circuit designers handwork.

In the rest of this section we will develop two transconductance equations, one using classical means to handle short channel effects, and a similar equation based on the $\alpha$ power model [58] which proves to handle mobility and velocity saturation effects, even if aggravated by short channel. Comparison with simulations and the conventional transconductance model will also be presented using the 28 nm UTB FDSOI CMOS process.

### 3.2.1 The Classical Transconductance

We start our research with the EKV bulk-referenced drain-to-source current equation, which can be found in [42] and given by

$$v_P - v_{S,D} = \sqrt{1+4i_{f,r}} + ln\left(\sqrt{1+4i_{f,r}} - 1\right) - (1 + ln\,(2)) \tag{3.16}$$

where $v_P$ is the normalized ($V_P/U_t$) pinch-off voltage defined in [38] and given by

$$v_P = \frac{v_G - v_T}{n}, \tag{3.17}$$

$i_{f,r}$ is the normalized forward (reverse) current given by

$$i_{f,r} = \frac{I_{f,r}}{I_{spec}}, \tag{3.18}$$

$v_{S,D}$ is the source (or drain) normalized voltage, $n$ is the slope factor, $v_G$ is the normalized gate voltage, $v_T$ is the normalized threshold voltage, $I_{f,r}$ is the forward (reverse) current and $I_{spec}$ is the transistor specific current.

In order to obtain the transistor transconductance applicable for every inversion level, an implicit first order derivative is applied in (3.16). The algebraic calculations are demonstrated through (3.19) to (3.21)

$$\frac{d\left(\frac{v_G - v_T - n v_{S,D}}{n}\right)}{dv_G} = \frac{d\left(\sqrt{1+4i_{f,r}} + ln\left(\sqrt{1+4i_{f,r}} - 1\right) - (1 + ln\,(2))\right)}{dv_G} \tag{3.19}$$

$$\frac{1}{n} = \frac{2}{\sqrt{1+4i_{f,r}}}\frac{di_{f,r}}{dv_G} + \frac{1}{\sqrt{1+4i_{f,r}} - 1}\frac{2}{\sqrt{1+4i_{f,r}}}\frac{di_{f,r}}{dv_G} \tag{3.20}$$

$$\frac{di_{f,r}}{dv_G} = \frac{1}{n}\frac{\left(\sqrt{1+4i_{f,r}} - 1\right)}{2}. \tag{3.21}$$

Equation (3.21) can be further simplified assuming saturation. This is a reasonable assumption for many applications where the transistors source is connected to the ground, or to $V_{DD}$ for the $p$-type, and the drain runs most of its transient far from its supply voltage values by at least about 100 mV. The resulting transconductance for saturation is given by

$$\frac{di_{ds}}{dv_G} = \frac{1}{n}\frac{\left(\sqrt{1+4i_f} - 1\right)}{2}. \tag{3.22}$$

We now denormalize (3.22), resulting in

$$\frac{dI_{ds}}{dV_G} = \frac{I_{spec}}{2nU_t}\left(\sqrt{1+4i_f} - 1\right) \tag{3.23}$$

where $U_t$ is the thermal voltage value at 27 °C.

The resulting transconductance (3.23) has little use for circuit design handwork since it is an implicit function of the gate voltage. In order to eliminate the transistor current and obtain the transconductance as an explicit function of the gate voltage, we plug the interpolated current function provided by [54] for saturated operation (3.24), which is given by

$$i_{ds} = ln^2\left(1 + exp\left(\frac{V_{GS} - V_T}{2nU_t}\right)\right) \tag{3.24}$$

into (3.23), leading to

$$\frac{dI_{DS}}{dV_{GS}} = \frac{I_{spec}}{2nU_t}\left(\sqrt{1 + 4ln^2\left(1 + exp\left(\frac{V_{GS} - V_T}{2nU_t}\right)\right)} - 1\right). \tag{3.25}$$

Observe that the substitution of (3.24) into (3.23) is only possible if bulk and source are short-connected because the bulk referenced and source referenced models turn out to have the same reference, allowing the straightforward shift between bulk and source referenced equations.

Charge sharing effects such as DIBL do have a strong influence in transistor drain-to-source current and, consequently, transconductance [21, 42]. As mentioned in Sec. 3.1, such effects are modeled by shifting the threshold voltage [21]. Hence (3.25) can be rewritten as

$$\frac{dI_{DS}}{dV_{GS}} = \frac{I_{spec}}{2nU_t}\left(\sqrt{1+4ln^2\left(1+exp\left(\frac{V_{GS}-V_T+\lambda V_{DS}}{2nU_t}\right)\right)}-1\right) \tag{3.26}$$

where $\lambda$ is a fitting parameter accounting for the DIBL effect.

### 3.2.2 The $\alpha$-power Like Transconductance

Short channel effects account for performance degradation in transistors with small length. Effects like DIBL, carrier mobility decrease and velocity saturation can be observed for voltages just above $V_T$. The sum of these facts lead to a reduced transconductance for high gate and drain voltages (does not need to be really high for short channel transistors) and otherwise for deep sub-threshold operations [21, 59].

In [60] it is proposed one way to get around short channel effects by adding another process parameter. To illustrate the idea proposed by [60], here is presented the transconductance equation provided by the ACM transistor model [61]

$$G_m = \frac{2}{1+\sqrt{1+\frac{I_{DS}}{I_{spec}}}} \times \frac{I_{DS}}{nU_t}. \tag{3.27}$$

This equation is as accurate as (3.23) however, [60] proposes to change the square root by any power $m$, usually between 1 and 0.5, which is used as a fitting parameter.

$$G_m = \frac{2}{1+\left(1+\frac{I_{DS}}{I_{spec}}\right)^m} \times \frac{I_{DS}}{nU_t}. \tag{3.28}$$

The idea behind this new parameter is that for $m$=0.5, the transconductance is the same as provided by the ACM model (3.27). For $m$=1, $G_m$ will no longer be a function of the bias current once it becomes sizable, saturating the transconductance at some gate voltage and not increasing anymore, which is exactly the behavior expected for severe carrier mobility and velocity saturation. The use of a fitting exponential parameter in order to model the effects mentioned in this section is well known and can find support in [58, 62–65].

We could use (3.27) nevertheless, we will not be consistent with the work developed so far which is based on the EKV model. In order to obtain a function which provides the same features of (3.28), we manipulate (3.23) as follows

$$\begin{aligned} G_m &= \frac{I_{spec}}{2nU_t}\left(\sqrt{1+4i_f}-1\right) = \frac{I_{DS}}{2nU_t}\frac{\left(\sqrt{1+4i_f}-1\right)}{i_f} \\ &= \frac{I_{DS}}{2nU_t}\frac{\left(\sqrt{1+4i_f}-1\right)}{i_f}\frac{\left(\sqrt{1+4i_f}+1\right)}{\left(\sqrt{1+4i_f}+1\right)} = \frac{I_{DS}}{nU_t}\frac{2}{1+\sqrt{1+4i_f}} \end{aligned} \tag{3.29}$$

Substituting the square root by the parameter proposed by [60], we obtain

$$G_m = \frac{2}{nU_t}\frac{I_{DS}}{1+(1+4i_f)^m}. \tag{3.30}$$

which holds the desired features of (3.28).

Once again, the transconductance as a implicit function of $V_{GS}$ is of little interest for this work so, we substitute (3.24) into (3.30), resulting in

$$G_m = \frac{I_{spec}}{nU_t}\frac{2ln^2\left(1+exp\left(\frac{V_{GS}-V_T}{2nU_t}\right)\right)}{1+\left(1+4ln^2\left(1+exp\left(\frac{V_{GS}-V_T}{2nU_t}\right)\right)\right)^m}. \tag{3.31}$$

Following the same procedure applied in (3.25) to (3.26), the threshold shift must be included in (3.31), leading to

$$G_m = \frac{I_{spec}}{nU_t}\frac{2ln^2\left(1+exp\left(\frac{V_{GS}-V_T+\lambda V_{DS}}{2nU_t}\right)\right)}{1+\left(1+4ln^2\left(1+exp\left(\frac{V_{GS}-V_T+\lambda V_{DS}}{2nU_t}\right)\right)\right)^m}. \tag{3.32}$$

In the following section, a comparison between (3.26) and (3.31) will be provided. The added parameter in (3.31) handles carrier mobility and velocity saturation.

### 3.2.3 Transconductance Comparison

In Figs. 3.23 and 3.24 can be found the simulated $n$-type regular $V_T$ small-signal transconductance and the fitted curves using (3.26) and (3.32) for $L$=80 nm and $L$=30 nm. Voltage $V_{DS}$ in both cases is 1 V (process voltage limit) for worst case short channel effects. The fitted $m$ in (3.32) and the mean and maximum errors for both equations can be found in Tabs. 3.16 and 3.17, respectively.

From Figs. 3.23 and 3.24 it is evident that (3.32) is more accurate than (3.26). Tab. 3.17 confirms it. Observe that (3.32) has clear advantage in strong inversion, where mobility saturation is achieved. Although, as mentioned in Sec. 3.1, the proposed model must hold for bias below 750 mV, (3.32) is a contribution so, we

challenged the proposed transconductance model with the FDSOI process bias limit, for that reason the illustrative Figs. 3.23 and 3.24 were simulated with $V_{GS}$ and $V_{DS}$ ranging from 0 V to 1 V.

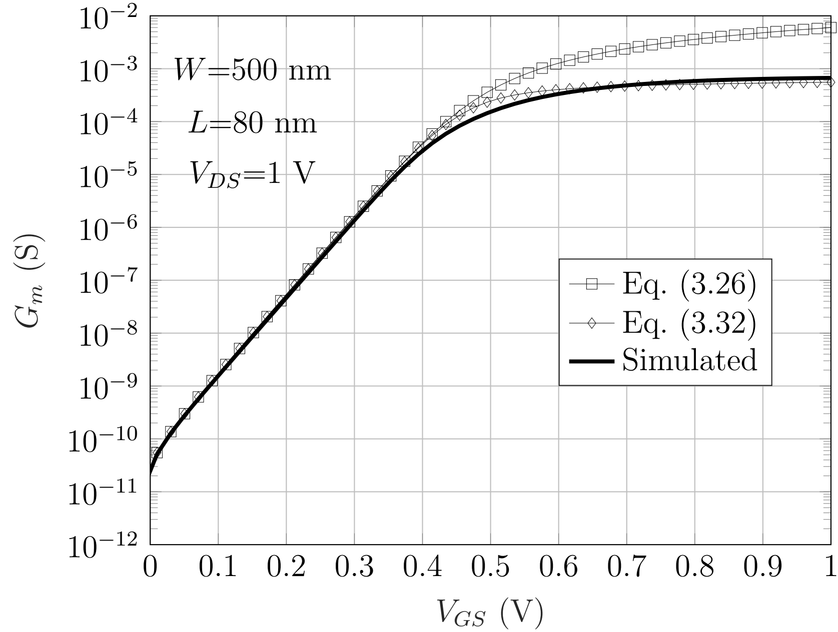


Figure 3.23: The $n$-type regular $V_T$ small-signal transconductance comparison among (3.26), (3.32) and simulation for $L$=80 nm.

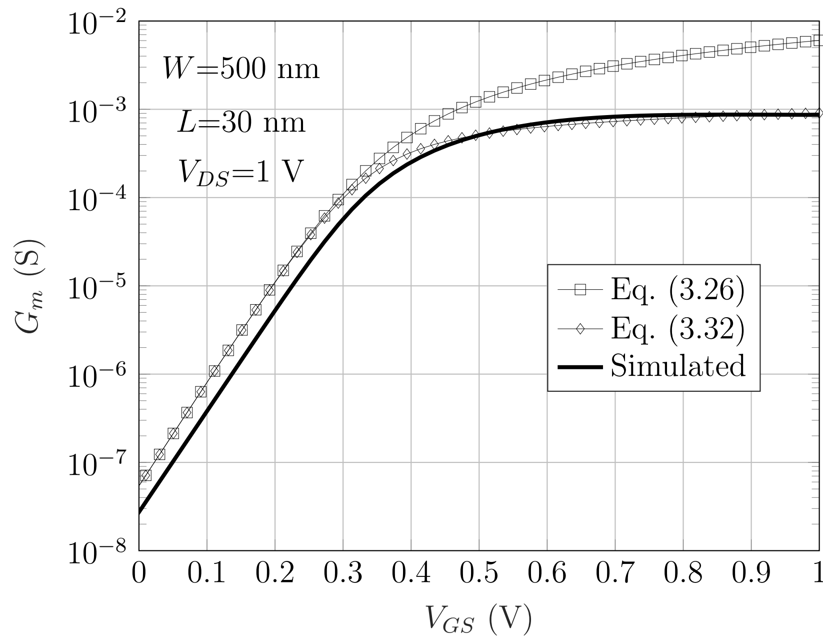


Figure 3.24: The $n$-type regular $V_T$ small-signal transconductance comparison among (3.26), (3.32) and simulation for $L$=30 nm.

From Tab. 3.17, one can observe that mean and maximum errors of (3.32) decrease with decreasing transistor length, on the other hand mean and maximum er-

Table 3.16: Fitted parameters of (3.32) used in Figs. 3.23 and 3.24.

| $L$ | $m$ |
|---|---|
| 80 nm | 0.9194 |
| 30 nm | 0.8367 |

Table 3.17: Mean and maximum error between simulations and fitted curves presented in Figs. 3.23 and 3.24.

| $L$ | (3.26) mean (%) | (3.26) max (%) | (3.32) mean (%) | (3.32) max (%) |
|---|---|---|---|---|
| 80 nm | 238.2 | 598.4 | 34.9 | 113.3 |
| 30 nm | 273.2 | 793.6 | 21.8 | 62.6 |

rors of (3.26) increase with decreasing $L$. The increasing error of (3.26) is explained by the threshold shift, which leads to current saturation for lower $V_{GS}$ compared with long channel transistor. The decreasing error of (3.32) has no physical background, it is entirely due to curve fitting procedure. Observe as well that $m$ decreased from $L$=80 nm to $L$=30 nm. This also has no physical background and is only justified by the curve fitting procedure as well.

The values for $m$ are obtained from a look up table generated from several simulations inside the region defined in Sec. 3.1.3 covered by $W$, $L$, $V_{GS}$ and $V_{DS}$. As mentioned, handling charge sharing effects by a constant term, $\lambda$, is a over simplification of the three dimensional nature of such effect also, among so many short-channel effects, channel modulation is not modeled by threshold shift or strong inversion transconductance slope change. Hence, for the sake of greater accuracy we add an extra parameter $\Gamma$ in (3.32) leading to

$$G_m = \Gamma \frac{I_{spec}}{nU_t} \frac{2ln^2\left(1+exp\left(\frac{V_{GS}-V_T+\lambda V_{DS}}{2nU_t}\right)\right)}{1+\left(1+4ln^2\left(1+exp\left(\frac{V_{GS}-V_T+\lambda V_{DS}}{2nU_t}\right)\right)\right)^m}. \tag{3.33}$$

Comparison between (3.33) and the simulated transconductance using the $n$-type regular $V_T$ transistor of the FDSOI process can be found in Figs. 3.25 and 3.26. Fitted parameters and mean and maximum errors are presented in Tabs. 3.18 and 3.19. Observe that (3.33) is more accurate than (3.32). In addition, parameter $m$ increases when $L$ decreases, which is physically consistent.

Table 3.18: Fitted parameters of (3.33) used in Figs. 3.25 and 3.26.

| $L$ | $\Gamma$ | $m$ |
|---|---|---|
| 80 nm | 0.5533 | 0.7029 |
| 30 nm | 0.7218 | 0.8350 |

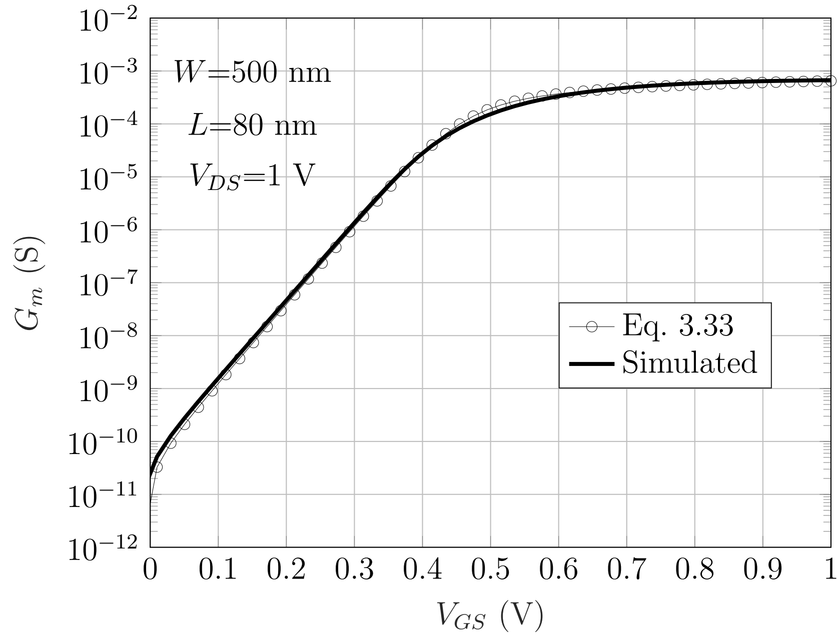


Figure 3.25: The $n$-type regular $V_T$ small-signal transconductance comparison between (3.33) and simulation for $L$=80 nm.

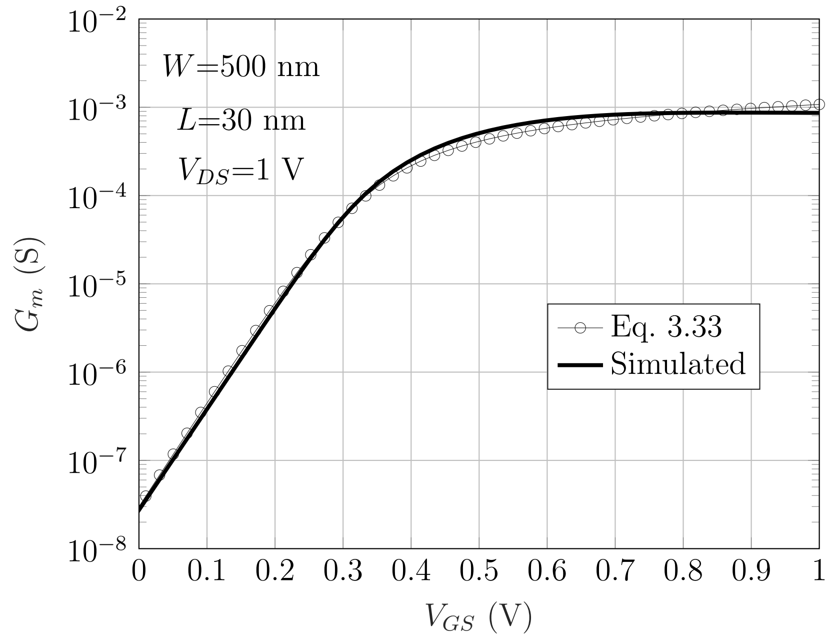


Figure 3.26: The $n$-type regular $V_T$ small-signal transconductance comparison between (3.33) and simulation for $L$=30 nm.

In the following subsection, (3.33) is used in order to extract the transconductance values for several corners inside the design region defined in Sec. 3.1.3.

Table 3.19: Mean and maximum errors between simulations and fitted curves presented in Figs. 3.25 and 3.26.

| $L$ | (3.33) mean error (%) | (3.33) maximum error (%) |
|---|---|---|
| 80 nm | 13.1 | 24.7 |
| 30 nm | 11.2 | 27.6 |

### 3.2.4 Extraction of $G_m$

In Figs. 3.27, 3.28, 3.29, 3.30, 3.31, 3.32, 3.33 and 3.34 can be found simulations and fitted curves for the corners of the design region defined in Sec. 3.1.3. The fitted parameters are presented in Tabs. 3.20, 3.21, 3.22 and 3.23. Mean and maximum error values for the presented simulations can be found in Tab. 3.24.

Observe from Figs. 3.27, 3.28, 3.29, 3.30, 3.31, 3.32, 3.33 and 3.34 that both simulations and the fitted curves using (3.33) are in close agreement, however, as observed in Tab. 3.24, mean errors can be up to 20% for the $n$-type and above 40% for the $p$-type for some transistor sizing and biasing. In order to justify such error, we refer back to the fitted curves in Figs. 3.23 and 3.24 using the EKV compact transconductance model given by (3.26), whose the fitted curve had mean errors above 200%. On top of that, (3.26) could not keep up with the simulated strong inversion saturation transconductance, leading to maximum errors up to 800%, therefore, both (3.33) and (3.32) turns out to be an improvement.

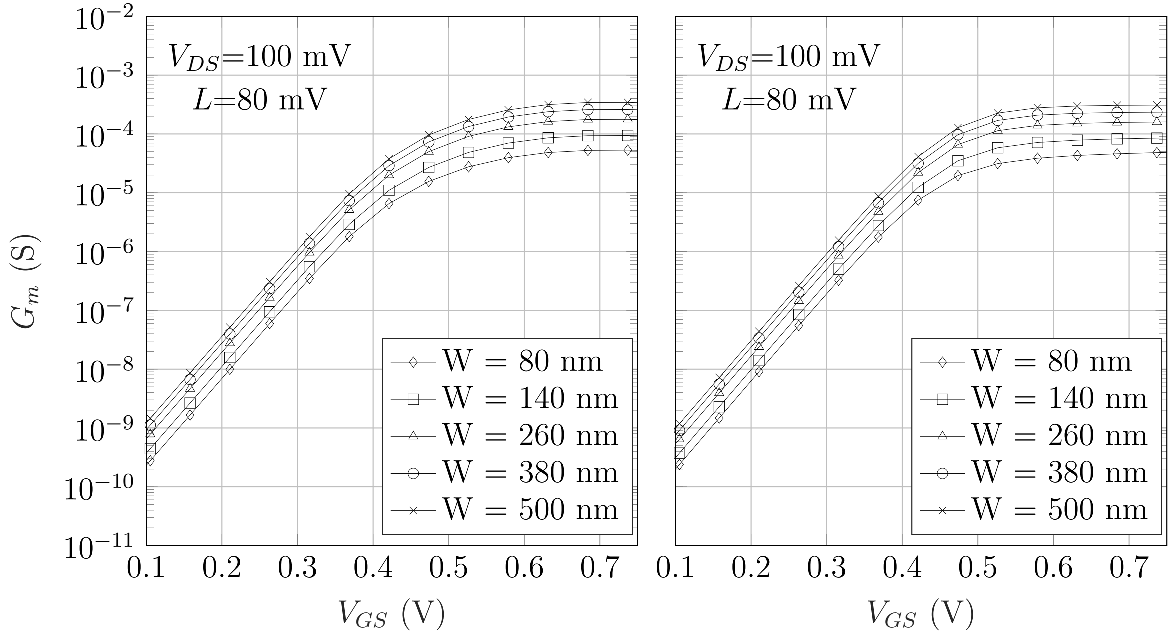


Figure 3.27: Simulated $n$-type regular $V_T$ small-signal transconductance behavior as a function $V_{GS}$ varying transistor width (left) and the fitted curve using (3.33) (right) for $L$=80 nm and $V_{DS}$=100 mV.

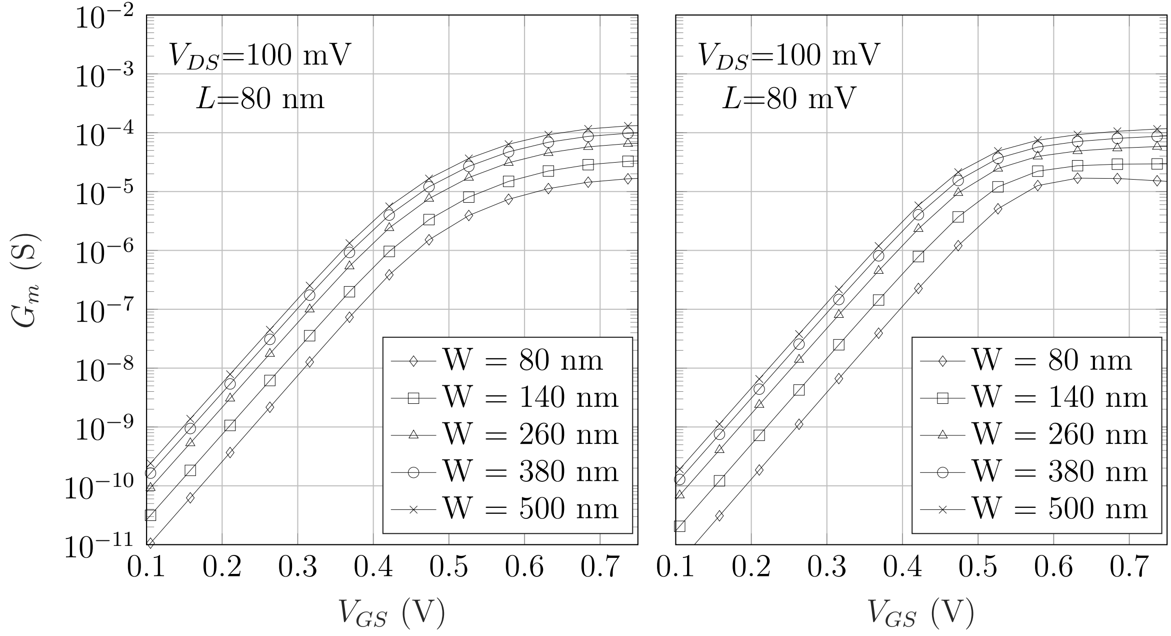


Figure 3.28: Simulated $p$-type low $V_T$ small-signal transconductance behavior as a function $V_{GS}$ varying transistor width (left) and the fitted curve using (3.33) (right) for $L$=80 nm and $V_{DS}$=100 mV.

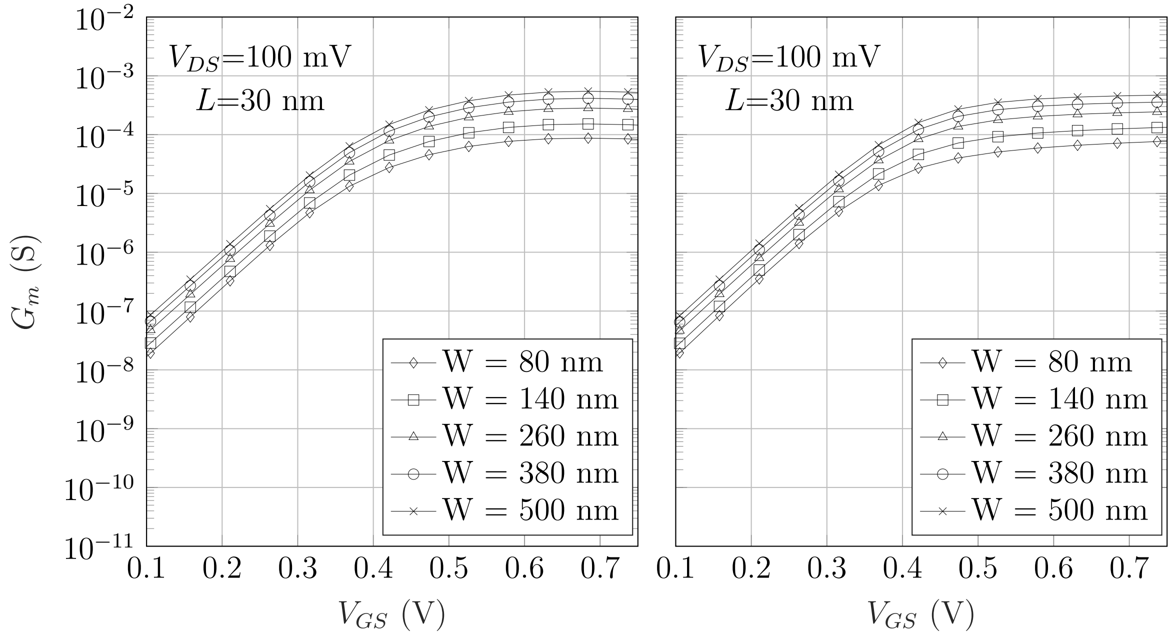


Figure 3.29: Simulated $n$-type regular $V_T$ small-signal transconductance behavior as a function $V_{GS}$ varying transistor width (left) and the fitted curve using (3.33) (right) for $L$=30 nm and $V_{DS}$=100 mV.

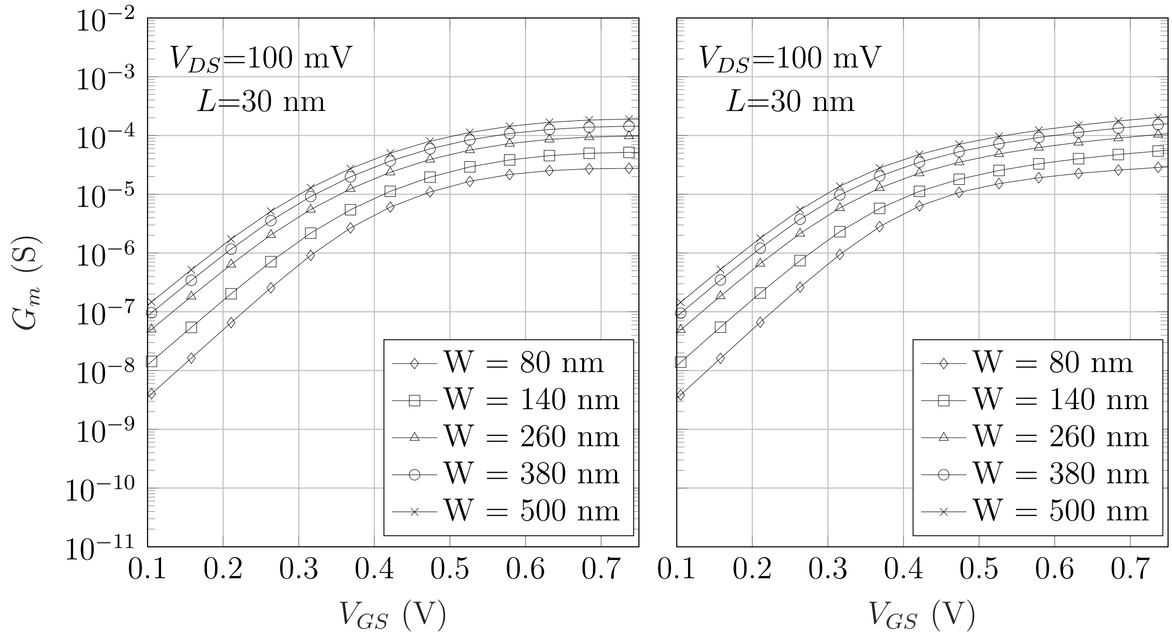


Figure 3.30: Simulated $p$-type low $V_T$ small-signal transconductance behavior as a function $V_{GS}$ varying transistor width (left) and the fitted curve using (3.33) (right) for $L$=30 nm and $V_{DS}$=100 mV.

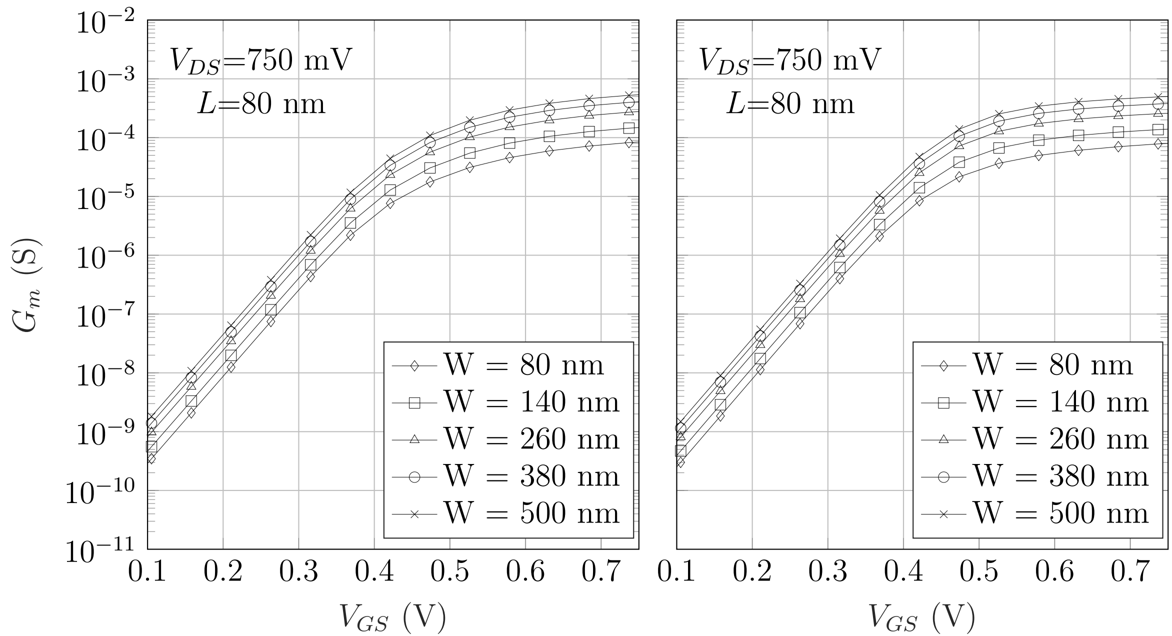


Figure 3.31: Simulated $n$-type regular $V_T$ small-signal transconductance behavior as a function $V_{GS}$ varying transistor width (left) and the fitted curve using (3.33) (right) for $L$=80 nm and $V_{DS}$=750 mV.

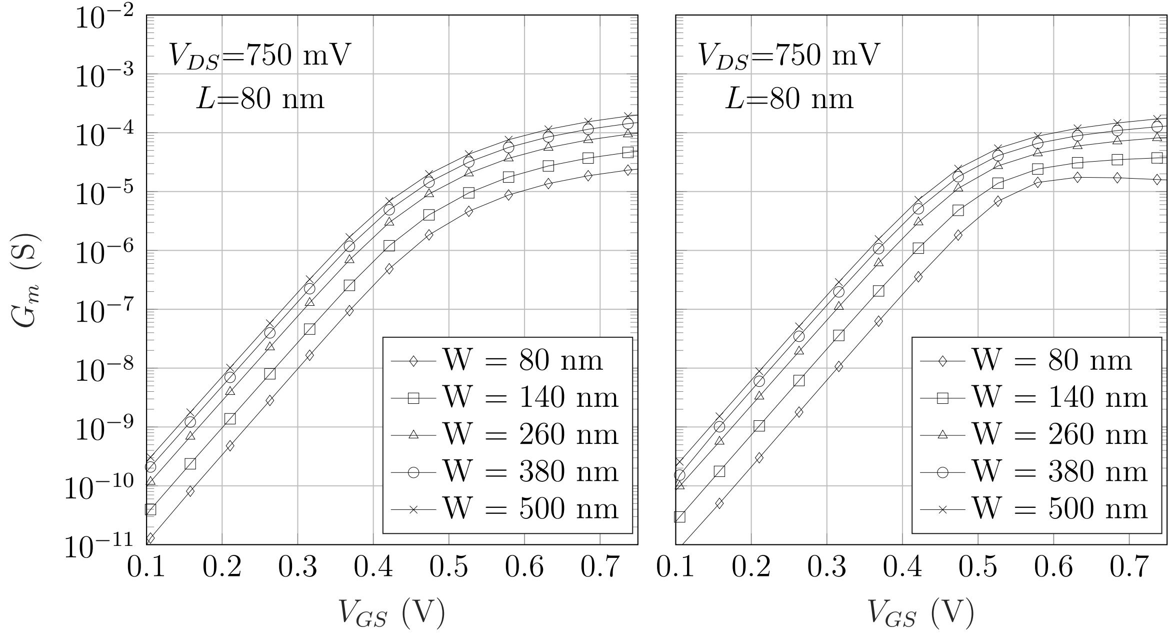


Figure 3.32: Simulated $p$-type low $V_T$ small-signal transconductance behavior as a function $V_{GS}$ varying transistor width (left) and the fitted curve using (3.33) (right) for $L$=80 nm and $V_{DS}$=750 mV.

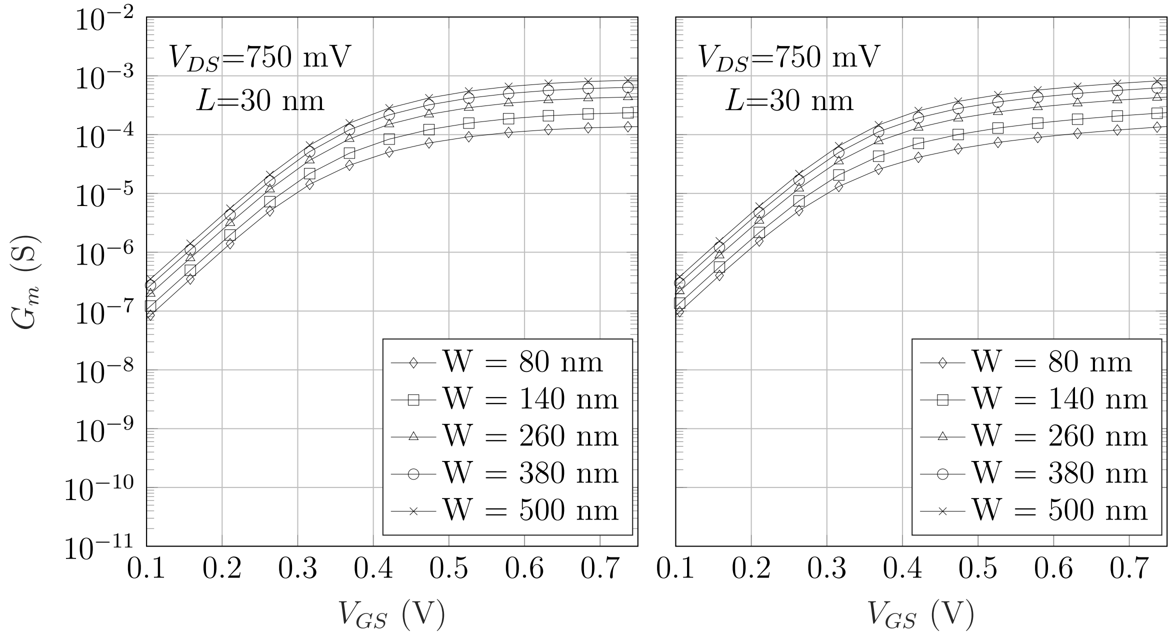


Figure 3.33: Simulated $n$-type regular $V_T$ small-signal transconductance behavior as a function $V_{GS}$ varying transistor width (left) and the fitted curve using (3.33) (right) for $L$=30 nm and $V_{DS}$=750 mV.

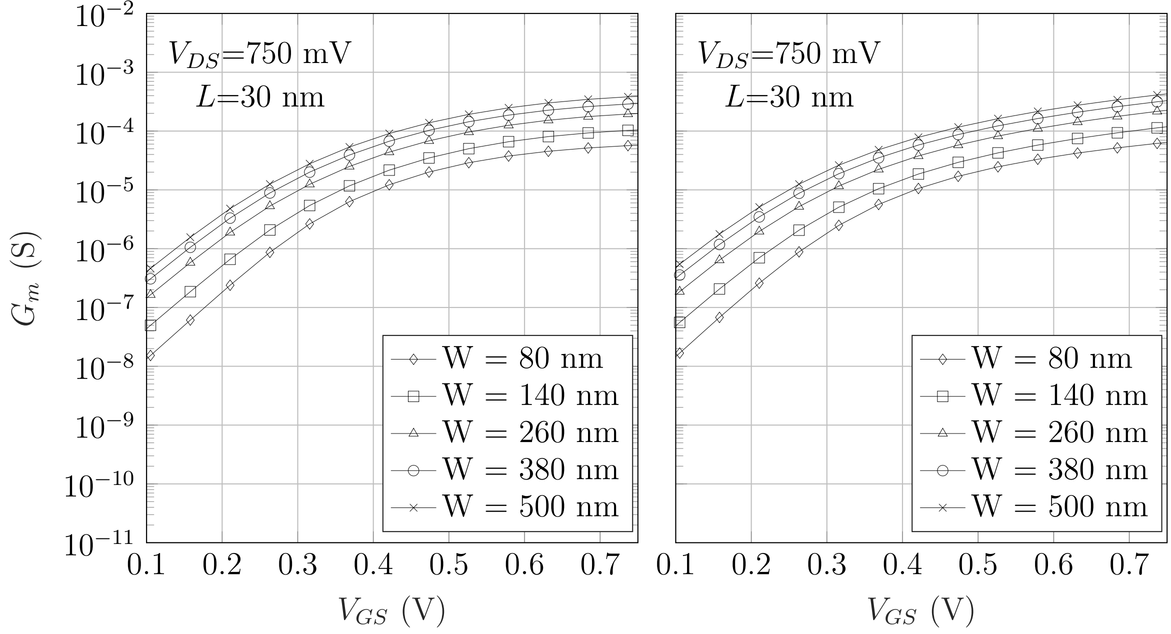


Figure 3.34: Simulated $p$-type low $V_T$ small-signal transconductance behavior as a function $V_{GS}$ varying transistor width (left) and the fitted curve using (3.33) (right) for $L$=30 nm and $V_{DS}$=750 mV.

Table 3.20: Fitted parameters of (3.33) used in Fig. 3.27 and 3.28.

| $W$ (nm) | $n$-type $\Gamma$ | $n$-type $m$ | $p$-type $\Gamma$ | $p$-type $m$ |
|---|---|---|---|---|
| 80 | 1.1310 | 0.7943 | 1.1469 | 0.7436 |
| 140 | 1.1192 | 0.8465 | 1.1495 | 0.6090 |
| 260 | 1.1073 | 0.8901 | 1.1444 | 0.5554 |
| 380 | 1.1015 | 0.9092 | 1.1424 | 0.5419 |
| 500 | 1.0981 | 0.9199 | 1.1415 | 0.5363 |

Table 3.21: Fitted parameters of (3.33) used in Fig. 3.29 and 3.30.

| $W$ (nm) | $n$-type $\Gamma$ | $n$-type $m$ | $p$-type $\Gamma$ | $p$-type $m$ |
|---|---|---|---|---|
| 80 | 1.0022 | 0.9103 | 0.6545 | 1.3414 |
| 140 | 0.9812 | 0.9528 | 0.8133 | 1.0900 |
| 260 | 0.9634 | 0.9862 | 0.9040 | 0.9449 |
| 380 | 0.9555 | 1.0004 | 0.9340 | 0.8946 |
| 500 | 0.9511 | 1.0082 | 0.9486 | 0.8692 |

Table 3.22: Fitted parameters of (3.33) used in Fig. 3.31 and 3.32.

| $W$ (nm) | $n$-type $\Gamma$ | $n$-type $m$ | $p$-type $\Gamma$ | $p$-type $m$ |
|---|---|---|---|---|
| 80 | 0.6374 | 0.5862 | 0.4935 | 0.4180 |
| 140 | 0.6287 | 0.6299 | 0.4566 | 0.2775 |
| 260 | 0.6212 | 0.6660 | 0.4293 | 0.2106 |
| 380 | 0.6178 | 0.6817 | 0.4187 | 0.1904 |
| 500 | 0.6158 | 0.6905 | 0.4132 | 0.1809 |

Table 3.23: Fitted parameters of (3.33) used in Fig. 3.27 and 3.28.

| $W$ (nm) | $n$-type $\Gamma$ | $n$-type $m$ | $p$-type $\Gamma$ | $p$-type $m$ |
|---|---|---|---|---|
| 80 | 0.8195 | 0.7770 | 0.5560 | 1.1753 |
| 140 | 0.8042 | 0.8188 | 0.6536 | 0.9342 |
| 260 | 0.7913 | 0.8515 | 0.7016 | 0.7905 |
| 380 | 0.7856 | 0.8654 | 0.7155 | 0.7395 |
| 500 | 0.7824 | 0.8731 | 0.7218 | 0.7135 |

Table 3.24: Mean and maximum error between simulations and fitted curves presented in Figs. 3.27, 3.28, 3.29, 3.30, 3.31, 3.32, 3.33 and 3.34.

| $L$=30 nm $V_{DS}$=100 mV | | | | |
|---|---|---|---|---|
| $W$ (nm) | $n$-type mean (%) | $n$-type max (%) | $p$-type mean (%) | $p$-type max (%) |
| 80 | 19.5 | 100.4 | 16.2 | 85.8 |
| 140 | 17.5 | 93.3 | 20.1 | 109.1 |
| 260 | 16.0 | 86.7 | 21.0 | 113.7 |
| 380 | 15.5 | 83.7 | 21.1 | 114.3 |
| 500 | 15.1 | 81.9 | 21.2 | 114.4 |
| $L$=80 nm $V_{DS}$=100 mV | | | | |
| $W$ (nm) | $n$-type mean (%) | $n$-type max (%) | $p$-type mean (%) | $p$-type max (%) |
| 80 | 13.1 | 37.9 | 43.3 | 73.5 |
| 140 | 13.4 | 30.7 | 27.2 | 51.7 |
| 260 | 13.8 | 31.8 | 17.4 | 42.5 |
| 380 | 14.0 | 32.6 | 15.9 | 36.9 |
| 500 | 14.1 | 32.9 | 15.6 | 33.7 |
| $L$=30 nm $V_{DS}$=750 mV | | | | |
| $W$ (nm) | $n$-type mean (%) | $n$-type max (%) | $p$-type mean (%) | $p$-type max (%) |
| 80 | 17.5 | 65.2 | 18.3 | 79.3 |
| 140 | 15.3 | 58.1 | 20.9 | 95.0 |
| 260 | 13.2 | 52.1 | 21.7 | 98.7 |
| 380 | 12.4 | 49.4 | 21.4 | 94.5 |
| 500 | 11.9 | 47.9 | 21.2 | 90.1 |
| $L$=80 nm $V_{DS}$=750 mV | | | | |
| $W$ (nm) | $n$-type mean (%) | $n$-type max (%) | $p$-type mean (%) | $p$-type max (%) |
| 80 | 8.8 | 21.8 | 44.6 | 110.9 |
| 140 | 10.9 | 25.1 | 30.6 | 130.5 |
| 260 | 12.5 | 27.3 | 24.9 | 179.5 |
| 380 | 13.2 | 28.2 | 25.6 | 242.3 |
| 500 | 13.6 | 28.6 | 28.2 | 319.2 |

## 3.3 Channel Conductance

In this section we develop a compact and yet accurate equation for $g_{ds}$. Simulations were carried out using the 28 nm UTBB FDSOI CMOS process. The design region defined by transistor sizes and bias conditions is the same as in Sec. 3.1.3. The model takes advantage of the concept of Early voltage [21, 66, 67], maintaining the EKV model for bias current. The resulting $g_{ds}$ model shows to be fairly accurate from weak to strong inversion and from triode to saturation region.

The remainder of this section is divided as follows. Section 3.3.1 investigates the $g_{ds}$ behavior through weak to strong inversion for the 28 nm UTBB FDSOI CMOS process. A study of the Early voltage is also advanced along with a small-signal conductance model. In Section 3.3.2 we carry on with the proposed model for $g_{ds}$, extraction and comparisons simulations are also presented. A compact analysis about the results is provided as well.

### 3.3.1 The Small-Signal Channel Impedance Model

The small-signal conductance definition is given by [21]

$$g_{ds} = \frac{dI_{ds}}{dV_{ds}}. \tag{3.34}$$

However, a more convenient model can be found in [21] as

$$g_{ds} = \frac{I_{DS}}{V_A} \tag{3.35}$$

where $I_{DS}$ is the transistor large-signal drain current and $V_A$ is the Early voltage.

The conductance equation in (3.35) is one of many ways to define $g_{ds}$ [68, 69]. In fact, since we have the parameters for an accurate drain current as used in the previous sections, we take advantage of this by using a small-signal conductance model which uses the explicit large signal drain current.

The modeling of the early voltage, $V_A$, imposes an obstacle to this thesis. We illustrate such difficulty in Figs. 3.35 and 3.36, where the $g_{ds}$ and $V_A^{-1}$ behaviors are presented, respectively. Both graphs were generated from simulations for the $n$-type regular $V_T$ for two different transistor sizes with similar aspect ratio and $V_{DS}$ fixed at 1 V for worst case short channel effects.

In Fig. 3.35 several differences can be observed between the curves. The horizontal shift is a clear evidence of a threshold voltage deviation, which is caused by charge sharing effects and DIBL. The second difference is exposed by the absence of the threshold voltage shift for transistors with longer channels, which leads to an increasing $g_{ds}$ for lower $V_{GS}$. This is explained by tunneling, which does not allow

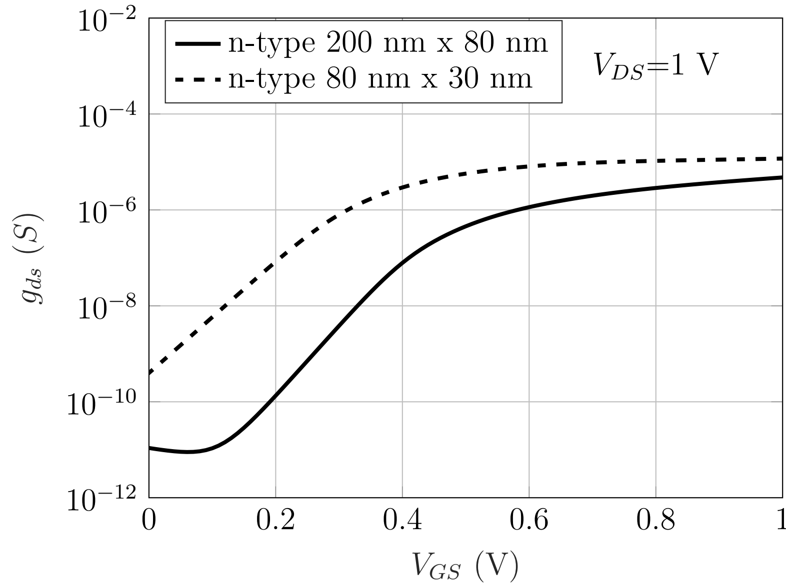


Figure 3.35: The $g_{ds}$ behavior for the $n$-type regular $V_T$ for two different transistor sizes.

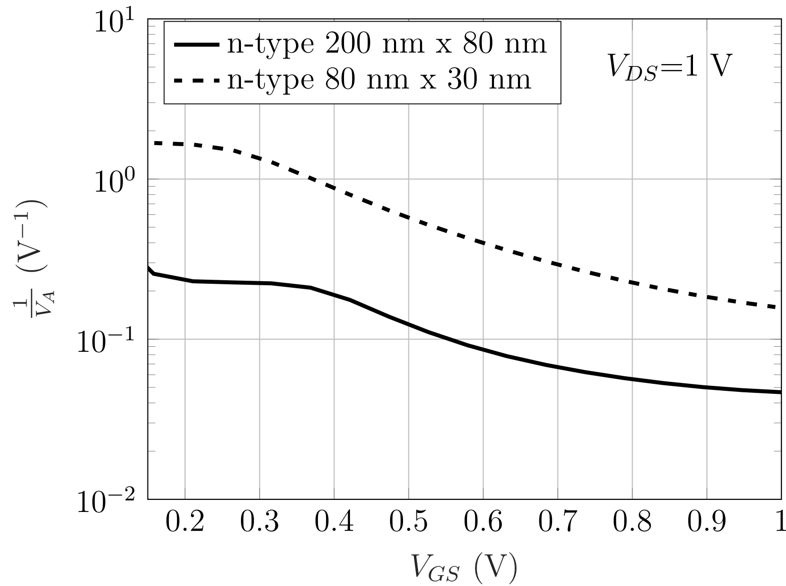


Figure 3.36: The $V_A^{-1}$ behavior for the $n$-type regular $V_T$ for two different transistor sizes.

drain current to decrease as the channel goes from depletion to accumulation as illustrated in Fig. 3.37. Since the voltage interval, where tunneling current becomes relevant, is small compared with the $V_{GS}$ range in the design region, we do not model such phenomenon, nevertheless we mentioned it for the sake of curiosity.

Both effects (DIBL and tunneling) can be observed in Fig. 3.36 as well. From (3.34), the threshold voltage shift due to DIBL ($\lambda$) can be pulled out from inside the bias current equation, shifting the Early voltage lower values (or higher values for $V_A^{-1}$). Tunneling also affects the shape of the Early voltage, however, we omitted

such phenomenon in Fig. 3.36 by plotting $V_A^{-1}$ from 150 mV and not from 0 V.

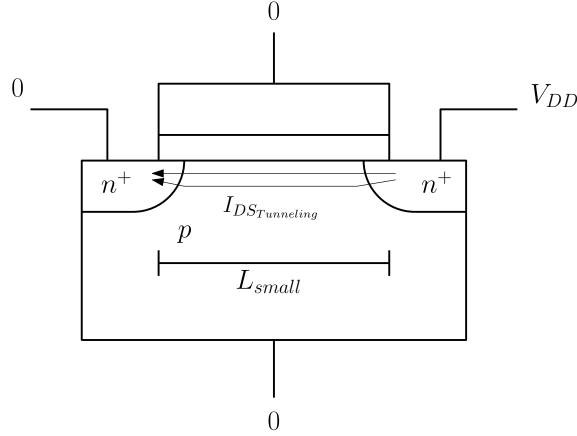


Figure 3.37: Leakage current illustration.

The classical $g_{ds}$ model from SPICE level 1 and 2 only accounts for channel length modulation in $V_A$, which is an oversimplification for short-channel transistors. Some works propose better models for $V_A$ for instance, work [67] proposes a fully empirical equation as a function of the inversion level. In [66] a physically based equation for Early voltage is developed, and DIBL and channel length modulation contributions are modeled individually. Both models do not prove to be accurate for transistors with very short channels. On top of that, several fitting parameters are needed. For greater accuracy, we propose an empirical equation for the Early voltage for the process under study. Fitting parameters and relative errors with simulations are provided next.

### The Proposed Early Voltage

When one tries to apply the small-signal conductance given by (3.35) in all inversion levels and for small transistors, the suitable Early voltage might become very complex. In order to propose an equation for $V_A$, we first study the Early voltage behavior. In Fig. 3.36 one can observe a plateau for $V_{GS} \ll V_{DS}$ and another one for $V_{GS} \approx V_{DS}$ (with $V_{DS}$=1 V). Between both plateaus (Fig. 3.38), a steadily decline can be observed between both plateaus, we propose to link those plateaus by a straight line (an exponential decline in a linear axis). In order to preserve the weak/moderate inversion behavior observed in Fig. 3.36 several different equations were tested, the one which had the best result is given by

$$\frac{1}{V_A} = a_0 + a_1 \left( 1 + \frac{\sqrt{1 + 4ln^2 \left(1 + exp\left(\frac{V_{GS}+a_2}{a_3}\right)\right)} + 1}{ln^{a_4}\left(1 + exp\left(\frac{V_{GS}+a_2}{a_3}\right)\right) + 1} \right)^{-1} \tag{3.36}$$

where $a_0$, $a_1$, $a_2$, $a_3$ and $a_4$ are fitting parameters.

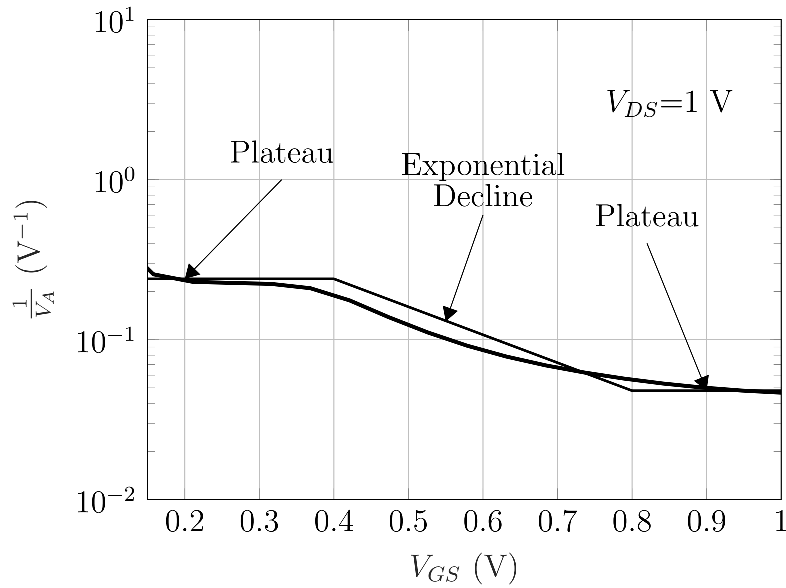


Figure 3.38: Illustration of both plateaus and the exponential slope of $V_A^{-1}$ obtained for the $n$-type regular $V_T$ transistor.

The idea behind (3.36), in order to model $g_{ds}$, arises from (3.12), where $C_{gs}$ has also two plateaus with a ramp up or ramp down between them. With the five parameters to be fitted in (3.36), the slope between both plateaus can be adjusted. For illustration, the curve in Fig. 3.38 is fitted by (3.36) in Fig. 3.39.

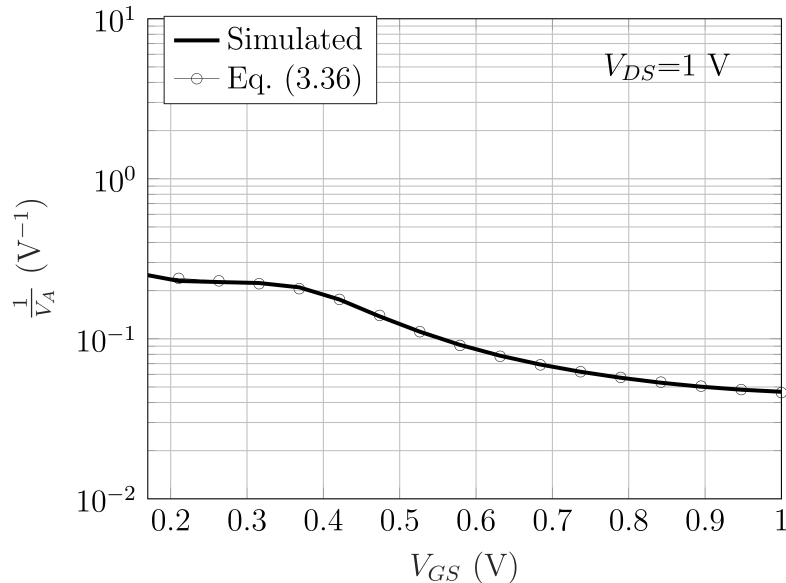


Figure 3.39: Inverse of the Early voltage behavior for the 200 $x$ 80 nm $n$-type regular $V_T$ and the fitted curve using (3.36).

Observe that $V_{DS}$ is not explicit in (3.36), therefore the fitted parameters account for bias. As it is demonstrated in Sec. 3.3.2, the parameters in (3.36) showed to be

reasonably constant with $W$, however, strongly affected by $V_{DS}$ and $L$ due to short channel effects.

### 3.3.2 Extraction of $g_{ds}$

For the extraction of $g_{ds}$, we follow the same procedure used for the extraction of the capacitances and transconductances in Secs. 3.1 and 3.2. In Figs. 3.40, 3.41, 3.42, 3.43, 3.44, 3.45, 3.46 and 3.47 can be observed simulations and fitted curves for the corners of the region defined in Sec. 3.1.3. In the same way as in Secs. 3.1 and 3.2 it is assumed that, if good accuracy is obtained at the design region corners, everywhere inside the design region must be accurate as well. The fitted parameters are presented in Tabs. 3.25, 3.26, 3.27, 3.28, 3.29, 3.30, 3.31 and 3.32. Mean and maximum errors for the presented simulations can be found in Tab. 3.33. The low-voltage $g_{ds}$ value difference between Figs. 3.40, 3.41, 3.42, 3.43 and Figs. 3.44, 3.45, 3.46, 3.47 points out that the DIBL effect is severe in short channel transistors. Observe the weak-inversion $g_{ds}$ value difference between the simulations for transistors with $L$=30 nm (Figs. 3.42, 3.43, 3.46 and 3.47) and $L$=80 nm (Figs. 3.40, 3.41, 3.44 and 3.45). Such phenomenon is in agreement with theory, in fact not only DIBL, but charge sharing, velocity overshoot, punchthrough and other effects, make the short channel easily pierced by electrons even if the transistor $V_{GS}$ is at 0 V, hence increasing the channel conductance.

From Figs. 3.40, 3.41, 3.42, 3.43, 3.44, 3.45, 3.46 and 3.47 we observe that both simulations and fitted curves using (3.36) are in close agreement. Mean errors remained bellow 46% for all simulations as indicated in Tab. 3.24. Observe that mean errors increases with short channel effects (lower $L$ and higher $V_{DS}$). This suggests that better refinement on the $g_{ds}$ model should be advanced. As suggested in Sec. 3.3.1 we stated that the fitted parameters would account for $V_{DS}$ and $L$, indeed, this is verified for the fitted parameters for both $n$-type (Tabs. 3.25, 3.27, 3.29 and 3.29) and $p$-type (Tabs. 3.26, 3.28, 3.30 and 3.30). At the very least, obtaining $g_{ds}$ by using a look up table is faster than by simulation. Nevertheless, it will cost the predictability of the $g_{ds}$ behavior for $V_{DS}$ and $L$ values outside the design region.

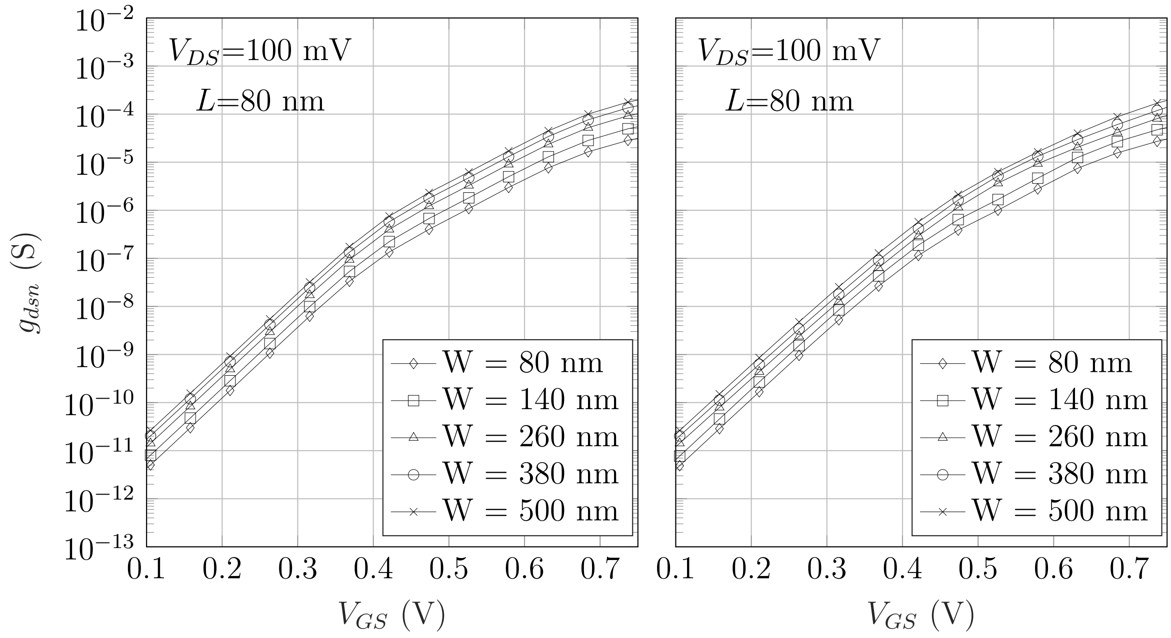


Figure 3.40: Simulated $n$-type low $V_T$ small-signal $g_{ds}$ behavior as a function of $V_{GS}$ varying transistor width (left) and the fitted curve using (3.36) (right) for $L$=80 nm and $V_{DS}$=100 mV.

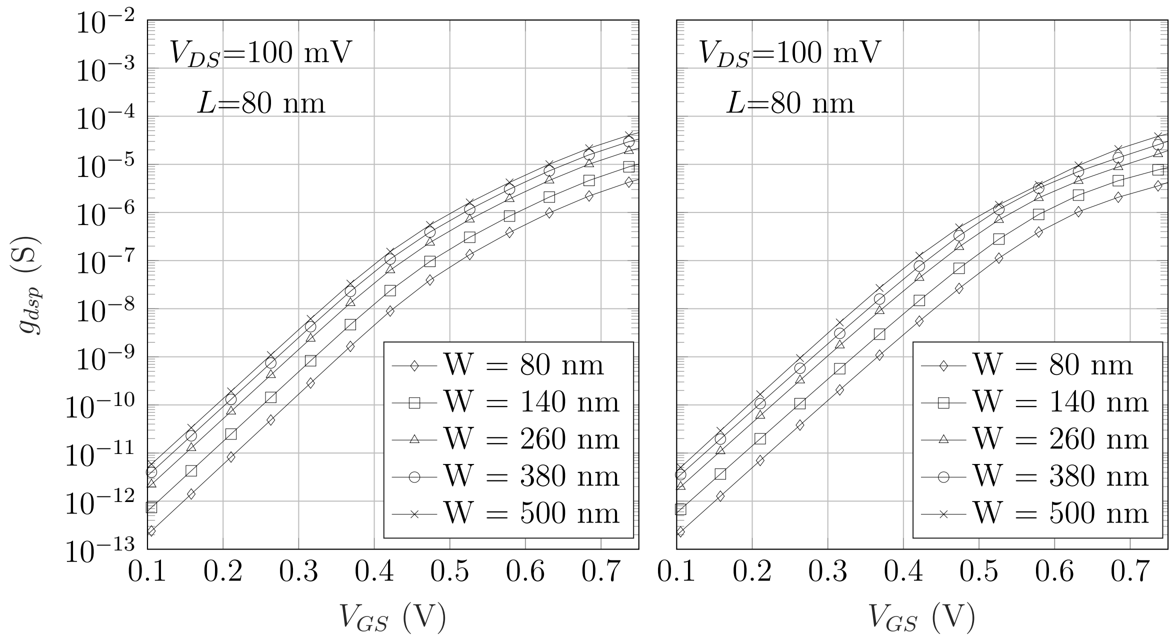


Figure 3.41: Simulated $p$-type low $V_T$ small-signal $g_{ds}$ behavior as a function of $V_{GS}$ varying transistor width (left) and the fitted curve using (3.36) (right) for $L$=80 nm and $V_{DS}$=100 mV.

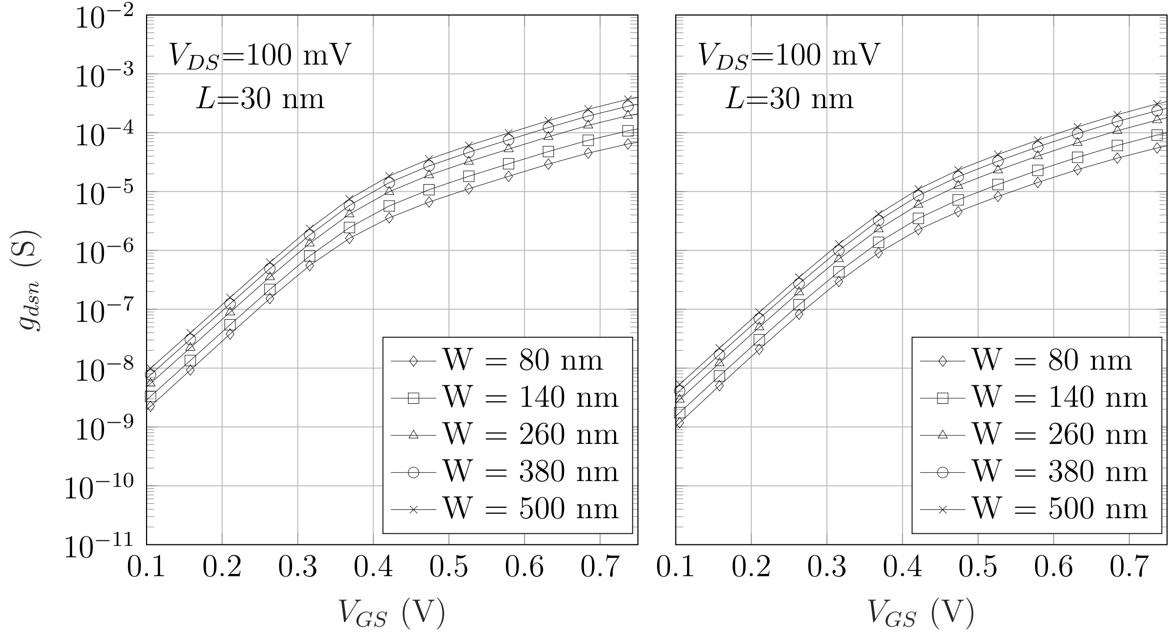


Figure 3.42: Simulated $n$-type low $V_T$ small-signal $g_{ds}$ behavior as a function of $V_{GS}$ varying transistor width (left) and the fitted curve using (3.36) (right) for $L$=30 nm and $V_{DS}$=100 mV.

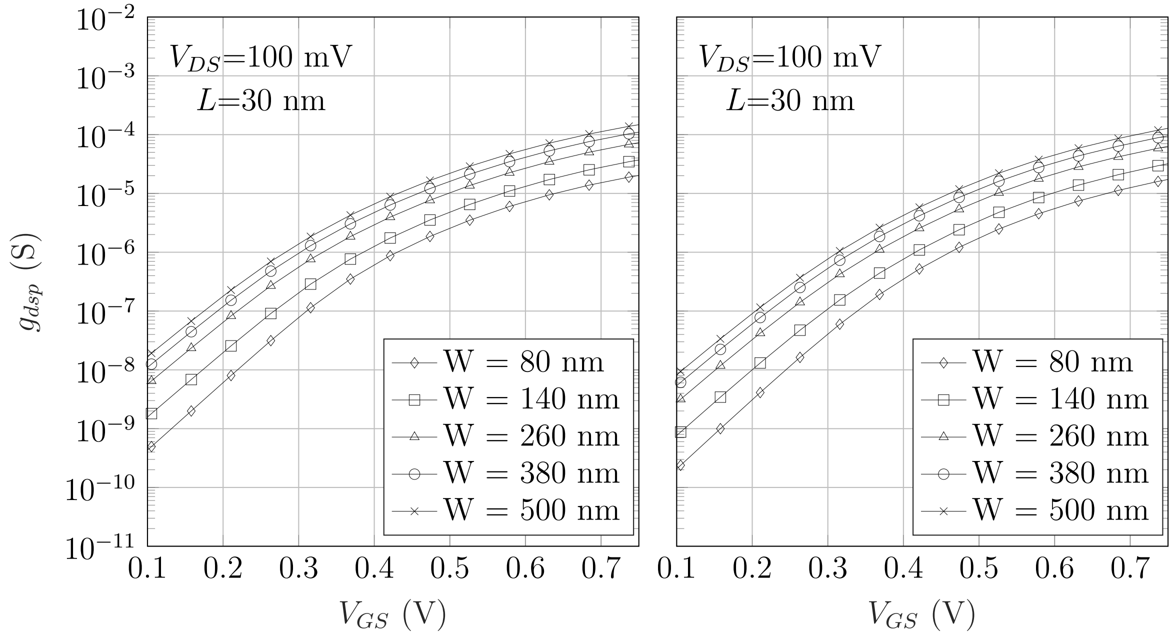


Figure 3.43: Simulated $p$-type low $V_T$ small-signal $g_{ds}$ behavior as a function of $V_{GS}$ varying transistor width (left) and the fitted curve using (3.36) (right) for $L$=30 nm and $V_{DS}$=100 mV.

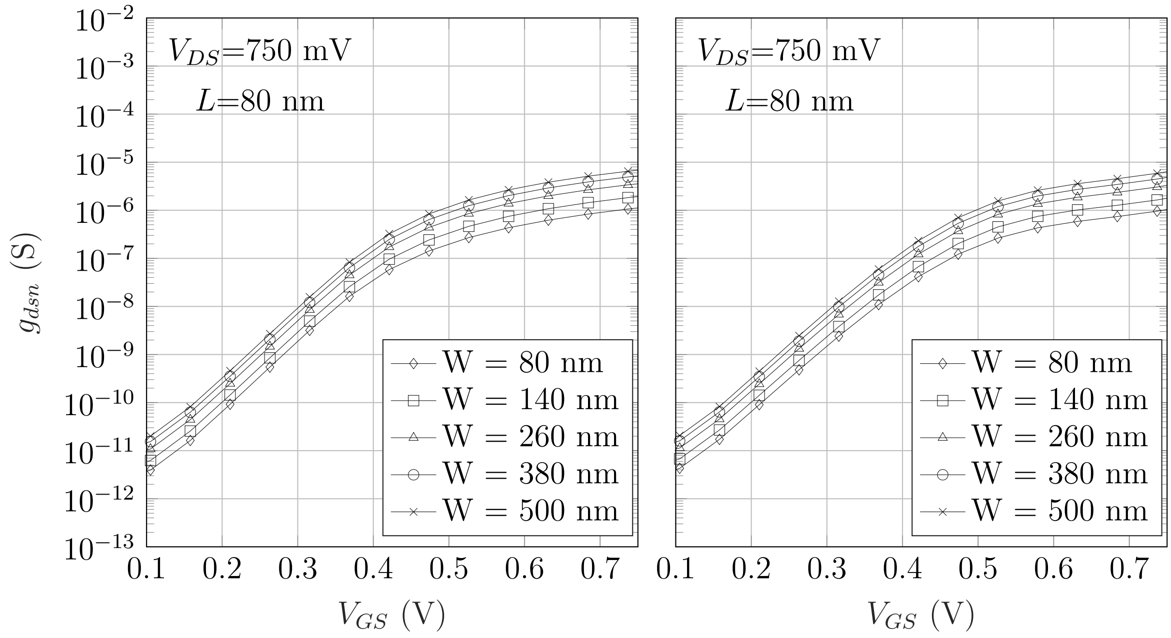


Figure 3.44: Simulated $n$-type low $V_T$ small-signal $g_{ds}$ behavior as a function of $V_{GS}$ varying transistor width (left) and the fitted curve using (3.36) (right) for $L$=80 nm and $V_{DS}$=750 mV.

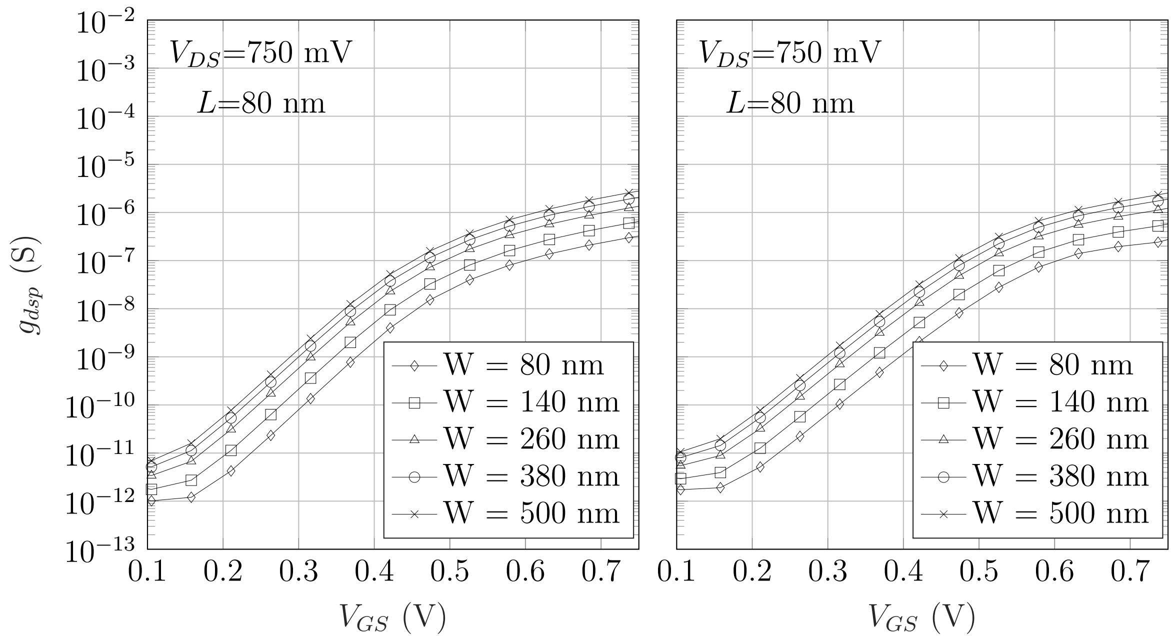


Figure 3.45: Simulated $p$-type low $V_T$ small-signal $g_{ds}$ behavior as a function of $V_{GS}$ varying transistor width (left) and the fitted curve using (3.36) (right) for $L$=80 nm and $V_{DS}$=750 mV.

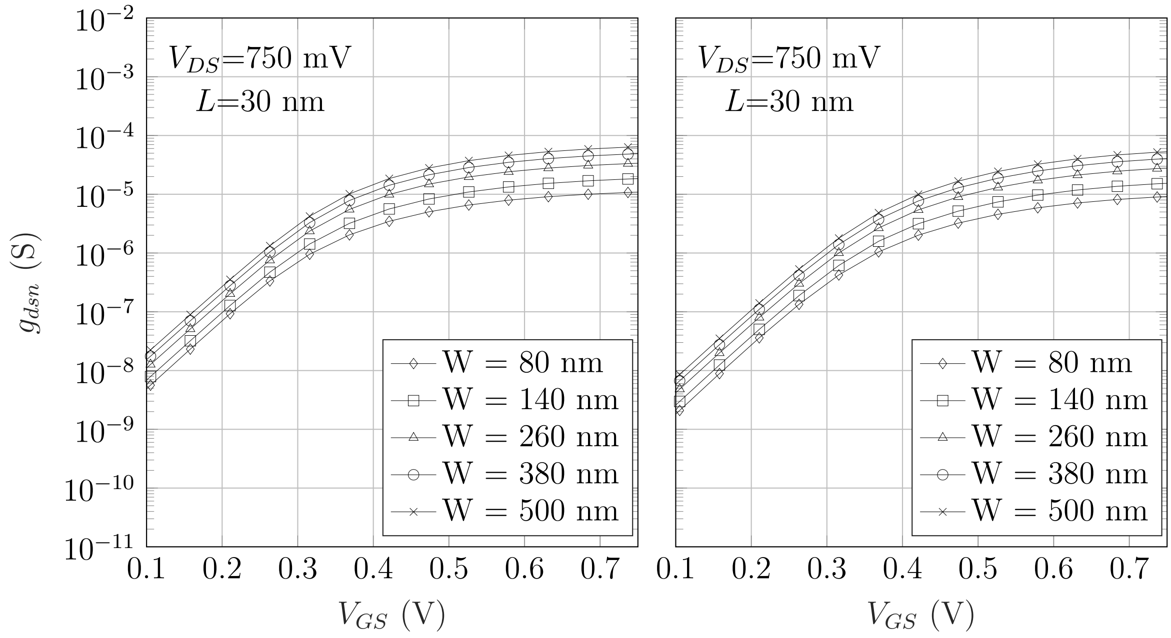


Figure 3.46: Simulated $n$-type low $V_T$ small-signal $g_{ds}$ behavior as a function of $V_{GS}$ varying transistor width (left) and the fitted curve using (3.36) (right) for $L$=30 nm and $V_{DS}$=750 mV.

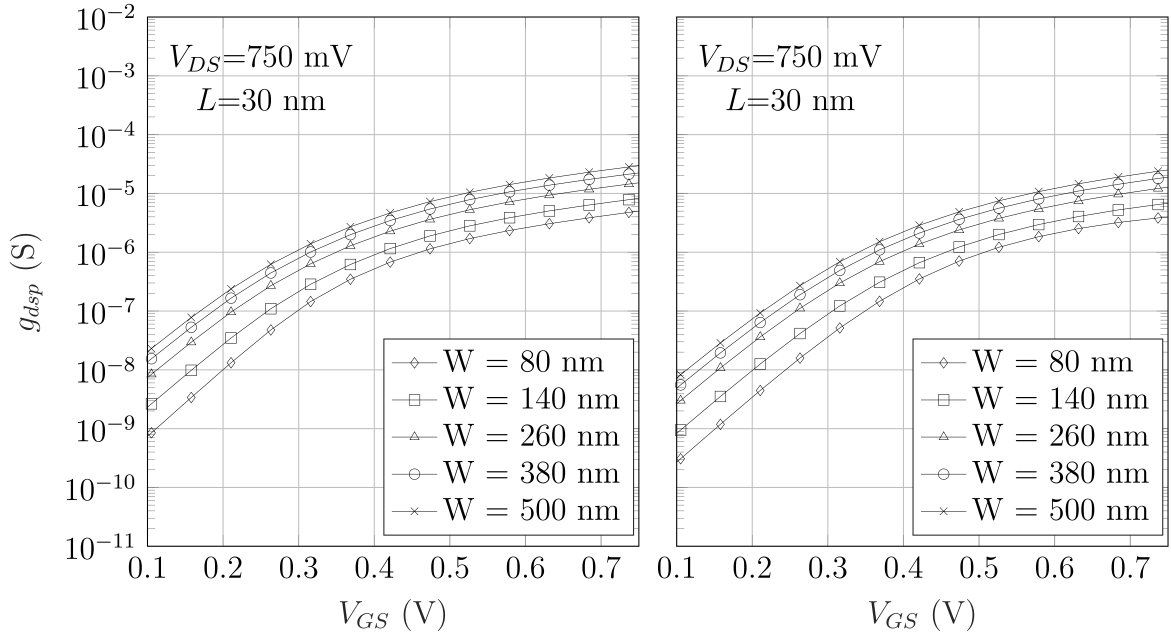


Figure 3.47: Simulated $p$-type low $V_T$ small-signal $g_{ds}$ behavior as a function of $V_{GS}$ varying transistor width (left) and the fitted curve using (3.36) (right) for $L$=30 nm and $V_{DS}$=750 mV.

Table 3.25: Fitted parameters of (3.36) used in Fig. 3.40.

| $W$ (nm) | $a_0$ | $a_1$ | $a_2$ | $a_3$ | $a_4$ |
|---|---|---|---|---|---|
| 80 | 0.9430 | -2.4188 | -0.5666 | 0.1654 | 0.0427 |
| 140 | 0.8783 | -2.3494 | -0.5593 | 0.2233 | 0.0444 |
| 260 | 0.8449 | -2.3358 | -0.5527 | 0.2746 | 0.0459 |
| 380 | 0.8339 | -2.3347 | -0.5498 | 0.2970 | 0.0465 |
| 500 | 0.8285 | -2.3346 | -0.5482 | 0.3095 | 0.0468 |

Table 3.26: Fitted parameters of (3.36) used in Fig. 3.41.

| $W$ (nm) | $a_0$ | $a_1$ | $a_2$ | $a_3$ | $a_4$ |
|---|---|---|---|---|---|
| 80 | 0.9321 | -2.4541 | -0.5215 | 0.8106 | 0.0550 |
| 140 | 0.9599 | -2.5277 | -0.5313 | 0.6741 | 0.0538 |
| 260 | 0.9888 | -2.5380 | -0.5498 | 0.4991 | 0.0507 |
| 380 | 1.0056 | -2.4967 | -0.5597 | 0.4119 | 0.0480 |
| 500 | 1.0171 | -2.4606 | -0.5653 | 0.3624 | 0.0462 |

Table 3.27: Fitted parameters of (3.36) used in Fig. 3.42.

| $W$ (nm) | $a_0$ | $a_1$ | $a_2$ | $a_3$ | $a_4$ |
|---|---|---|---|---|---|
| 80 | 3.9509 | -10.5239 | -0.4538 | 0.6975 | 0.0673 |
| 140 | 3.8343 | -10.1650 | -0.4555 | 0.7392 | 0.0634 |
| 260 | 3.7604 | -9.9347 | -0.4569 | 0.7667 | 0.0607 |
| 380 | 3.7329 | -9.8497 | -0.4576 | 0.7770 | 0.0597 |
| 500 | 3.7185 | -9.8058 | -0.4580 | 0.7823 | 0.0591 |

Table 3.28: Fitted parameters of (3.36) used in Fig. 3.43.

| $W$ (nm) | $a_0$ | $a_1$ | $a_2$ | $a_3$ | $a_4$ |
|---|---|---|---|---|---|
| 80 | 4.2682 | -8.9436 | -0.4365 | 0.8119 | 0.0848 |
| 140 | 4.4031 | -8.7396 | -0.4351 | 0.6101 | 0.0921 |
| 260 | 4.4700 | -8.5652 | -0.4307 | 0.4752 | 0.0865 |
| 380 | 4.4862 | -8.4905 | -0.4287 | 0.4317 | 0.0838 |
| 500 | 4.4916 | -8.4441 | -0.4275 | 0.4111 | 0.0824 |

Table 3.29: Fitted parameters of (3.36) used in Fig. 3.44.

| $W$ (nm) | $a_0$ | $a_1$ | $a_2$ | $a_3$ | $a_4$ |
|---|---|---|---|---|---|
| 80 | 0.3567 | -1.2584 | -0.4772 | 0.6986 | 0.1204 |
| 140 | 0.3112 | -1.0283 | -0.4643 | 0.7602 | 0.0969 |
| 260 | 0.2904 | -0.9208 | -0.4591 | 0.7941 | 0.0848 |
| 380 | 0.2838 | -0.8866 | -0.4577 | 0.8056 | 0.0807 |
| 500 | 0.2806 | -0.8698 | -0.4570 | 0.8114 | 0.0787 |

Table 3.30: Fitted parameters of (3.36) used in Fig. 3.45.

| $W$ (nm) | $a_0$ | $a_1$ | $a_2$ | $a_3$ | $a_4$ |
|---|---|---|---|---|---|
| 80 | 0.2782 | -0.8167 | -0.4919 | 0.8554 | 0.0533 |
| 140 | 0.2568 | -0.7343 | -0.4862 | 0.8524 | 0.0592 |
| 260 | 0.2372 | -0.6374 | -0.4790 | 0.8630 | 0.0600 |
| 380 | 0.2292 | -0.5949 | -0.4756 | 0.8681 | 0.0597 |
| 500 | 0.2250 | -0.5719 | -0.4737 | 0.8706 | 0.0595 |

Table 3.31: Fitted parameters of (3.36) used in Fig. 3.46.

| $W$ (nm) | $a_0$ | $a_1$ | $a_2$ | $a_3$ | $a_4$ |
|---|---|---|---|---|---|
| 80 | 1.0942 | -1.9628 | -0.3704 | 1.0616 | 0.0545 |
| 140 | 1.0610 | -2.0185 | -0.3813 | 1.0390 | 0.0524 |
| 260 | 1.0375 | -2.0586 | -0.3887 | 1.0231 | 0.0511 |
| 380 | 1.0282 | -2.0741 | -0.3915 | 1.0168 | 0.0506 |
| 500 | 1.0232 | -2.0823 | -0.3930 | 1.0135 | 0.0503 |

Table 3.32: Fitted parameters of (3.36) used in Fig. 3.47.

| $W$ (nm) | $a_0$ | $a_1$ | $a_2$ | $a_3$ | $a_4$ |
|---|---|---|---|---|---|
| 80 | 0.6849 | -0.8281 | -0.3902 | 1.1075 | 0.0524 |
| 140 | 0.5761 | -0.2553 | -0.3433 | 1.3546 | 0.0492 |
| 260 | 0.5061 | -0.0310 | -0.2884 | 1.7440 | 0.0257 |
| 380 | 0.4807 | -0.0032 | -0.2778 | 1.9725 | 0.0077 |
| 500 | 0.4670 | -0.0477 | -0.3594 | 1.6547 | 0.0618 |

Table 3.33: Mean and maximum error between simulations and fitted curves presented in Figs. 3.40, 3.41, 3.42, 3.43, 3.44, 3.45, 3.46 and 3.47.

| $L$=80 nm $V_{DS}$=100 mV | | | | |
|---|---|---|---|---|
| $W$ (nm) | $n$-type mean (%) | $n$-type max (%) | $p$-type mean (%) | $p$-type max (%) |
| 80 | 11.6 | 38.6 | 13.6 | 30.1 |
| 140 | 13.8 | 49.4 | 13.0 | 26.0 |
| 260 | 14.7 | 55.4 | 12.0 | 23.7 |
| 380 | 15.1 | 58.0 | 11.5 | 22.8 |
| 500 | 15.3 | 59.5 | 11.3 | 22.2 |
| $L$=30 nm $V_{DS}$=100 mV | | | | |
| $W$ (nm) | $n$-type mean (%) | $n$-type max (%) | $p$-type mean (%) | $p$-type max (%) |
| 80 | 31.1 | 52.9 | 31.1 | 56.4 |
| 140 | 31.5 | 52.2 | 30.1 | 56.2 |
| 260 | 31.8 | 51.8 | 29.1 | 55.5 |
| 380 | 31.9 | 51.6 | 28.9 | 54.7 |
| 500 | 32.0 | 51.5 | 28.8 | 54.6 |
| $L$=80 nm $V_{DS}$=750 mV | | | | |
| $W$ (nm) | $n$-type mean (%) | $n$-type max (%) | $p$-type mean (%) | $p$-type max (%) |
| 80 | 33.7 | 141.8 | 36.1 | 99.9 |
| 140 | 35.8 | 158.8 | 32.7 | 99.8 |
| 260 | 33.0 | 132.6 | 30.8 | 99.6 |
| 380 | 32.2 | 125.3 | 29.9 | 99.5 |
| 500 | 31.9 | 122.0 | 29.4 | 99.4 |
| $L$=30 nm $V_{DS}$=750 mV | | | | |
| $W$ (nm) | $n$-type mean (%) | $n$-type max (%) | $p$-type mean (%) | $p$-type max (%) |
| 80 | 42.2 | 69.5 | 40.7 | 70.7 |
| 140 | 42.7 | 67.9 | 39.0 | 69.8 |
| 260 | 44.5 | 69.1 | 37.7 | 69.0 |
| 380 | 45.3 | 75.5 | 37.2 | 68.6 |
| 500 | 45.7 | 78.7 | 36.6 | 68.3 |

## 3.4 Summary

Analytic models, valid for all inversion level of operations, for transistor small-signal capacitance, transconductance and channel conductance were proposed. Fitting parameters for the 28 nm UTBB FDSOI CMOS process are also provided. Simulations and fitted curves showed to be in close agreement with every model.

The challenging gate-to-source capacitance was very accurately modeled using only three fitting parameters. Mean errors were less than 12% at the design region corners. Other small-signal capacitances showed to be bias independent and were easily modeled with mean and maximum errors less than 2%.

The transconductance model was inspired in the $\alpha$-power model [58]. The addition of a fitting parameter to a classical transconductance equation proved to be a great improvement by providing better accuracy. Worst mean error was less than 20% for the $n$-type and less than 45% for the $p$-type, which is an improvement compared with the classical transconductance equation as observed in Figs. 3.23 and 3.24.

The proposed small-signal channel conductance model was fully mathematical. Worst mean error was about 45% for the $n$-type and up to 40% for the $p$-type. The proposed model has five fitting parameters which are strongly affected by $V_{DS}$ and $L$, a huge drawback. However, it provides accurate and fast $g_{ds}$ evaluation. On top of that, accurate and compact Early voltage model with a physical background is missing in literature. Therefore, comparing $g_{ds}$ models which use the Early voltage definition was not possible.

# Chapter 4

# Latch Design

In Chapter 1 we mentioned that the demand for fast, robust and low energy consuming digital circuits led to the inviability of hand work analysis. The use of sophisticated and complex models became the only, and computing demanding, way to evaluate digital circuit performance. In Chapter 2 we advanced a study of the latch circuit. By developing a small-signal analysis around the metastability voltage, we found out a linearized circuit which avoids the time consuming iterative small-signal calculation commonly used in recent circuit models such as BSIM. In Chapter 3 equations for evaluation of small-signal parameters such as capacitances, transconductance and channel conductance was developed. Apart from using a specific circuit architecture, some performance requirements can only be achieved with proper transistor sizing and defining a suitable supply voltage level. In order to establish a direct link between circuit performance and both transistor sizing and supply voltage level, every small-signal parameter was extracted as a function of transistor dimensions and bias. In this Chapter, we will assemble every model developed so far in a single cost function which will lead to the best compromise between speed and yield for the 7T-LTSA inside the design region defined in Chapter 3.

This Chapter is organized as follows. Section 4.1 will introduce the cost function. A convenient way of determining constant effective parameters will also be advanced. Equations to evaluate the latch input offset voltage and the metastability voltage will also be presented. Section. 4.2 presents the evaluation of the proposed time delay models and the cost function. Results using the developed equations and simulations will prove to be in close agreement, whereas, using the equations developed in this thesis will show to be several times faster. Section 4.2 will compare the latch optimized by the proposed approach for the 28 nm UTBB FDSOI CMOS process with some latch architectures found in recent works. Concluding remarks are made in Section. 4.4

## 4.1 The Cost Function

In [1] a complete 7T-LTSA latch analysis was carried out, an useful figure of merit was proposed relating input voltage level with yield and speed, (4.1), along with analytical and computational means to evaluate it. Since the input common mode voltage is directly proportional to delay and inversely proportional to yield [1], a compromise between delay and yield is achieved. The proposed figure of merit ranks such compromise and, ultimately, can be used as a cost function in order to find the best input voltage level:

$$FOM = \frac{Y(V_{INDC})}{t_d(V_{INDC})/t_{min}} \tag{4.1}$$

The drawback in [1] is that it fails to characterize latch behavior for near/sub-threshold operations, and therefore the proposed latch transient decision time delay equations in [1] are obsolete. Another problem is that the proposed yield evaluation is carried out by monte carlo simulations, which is the most computational hungry circuit analysis approach. We propose to replace (4.1) with

$$FOM = \frac{Y(W, L)}{t_d(W, L)/t_{min}} \tag{4.2}$$

where $t_{min}$ is now defined as the minimum delay for a given supply voltage and input voltage levels by varying transistor sizes.

### 4.1.1 The Metastability Voltage

The metastability voltage is the cornerstone of the dynamic equations developed in Chapter 2, so it goes without saying the need of an analytical equation for $V_S$. A good model for the inverter metastability voltage is proposed in [41]. If both inverters are perfectly matched, the corresponding metastability voltage value are equal and given by

$$V_S = \frac{V_{DD}}{2}(1 + \overline{\lambda}) + \frac{\overline{n}U_t}{2} log\left(\frac{\beta_p}{\beta_n}\right)(1 - \overline{\lambda}) \tag{4.3}$$

where

$$\beta_{n,p} = I_{specn,p} exp\left(\frac{V_{Tn,p}}{n_{n,p}U_t}\right) \tag{4.4}$$

$$\overline{n} = 2\frac{n_n n_p}{n_n + n_p} \tag{4.5}$$

$$\overline{\lambda} = \frac{\overline{n}}{2}\left(\frac{\lambda_p}{n_p} + \frac{\lambda_n}{n_n}\right) \tag{4.6}$$

where $I_{spec}$ is the transistor specific current, $V_T$ is threshold voltage value, $n$ is the slope factor, $\lambda$ is the DIBL effect, $V_{DD}$ the supply voltage level and $U_t$ is the thermal voltage. The subscripts $n$ and $p$ stand for either $n$ or $p$-type transistors, respectively.

### 4.1.2 The Effective Parameters

In Chapter 3 we stated the need for obtaining effective parameters as functions of transistors sizing instead of from curve fitting. In order to accomplish this goal, we will use the equations developed in Chapter 3 and take the average value across a bias interval. The integration intervals are not straightforward and need a good understanding of the latch behavior to be defined. In Fig. 4.1 we illustrate the bias intervals of both inverter drain voltages across a transient decision. At the center of the figure, the model developed in Sec. 2.3.3 can be observed for clarification on how the inverters output voltages are connected to the transistor small-signal parameters studied in Chapter 3.

In Sec. 2.2 we proposed to use two sets of small-signal effective parameters related to the discharging and regeneration phases in order to grasp a more accurate latch transient behavior. By means of obtaining two sets of effective parameters, two integration intervals must be defined. The integration intervals is presented in Fig. 4.1 for each inverter. It is important to note that the transistors of the inverters do communicate with each other. For example, if one effective transistor parameter is a result of a double integration of $V_{GS}$ and $V_{DS}$, the $V_{DS}$ interval is defined by the output voltage of the inverter to which the transistor belongs. On the other hand, $V_{GS}$ is defined by the output voltage of the other transistor.

#### Capacitances

Each load capacitance can be divided into other small-signal transistor parasitics of both inverters, as can be observed in Fig. 3.1 and in (3.2), (3.3) and (3.4). When the latch decision behavior was described in Sec. **??** we defined initial conditions for $V_1$ and $V_2$, such that as the inverter whose output voltage is $V_2$ goes to a high logic value at the end of the transient decision, i.e., winner inverter. We will keep such definition here, so that, every small-signal parameter with subscript 2 belongs to one of the transistors of the winner inverter. Otherwise, parameters with subscript 1 belongs to the loser inverter.

The gate-to-source capacitance proved to be strongly dependent on both $V_{GS}$ and $V_{DS}$, hence, the average $C_{gs}$ value must be taken by integrating (3.12) in both voltages. Observe that the gate-to-source capacitances at $V_2$, belong to the transistor

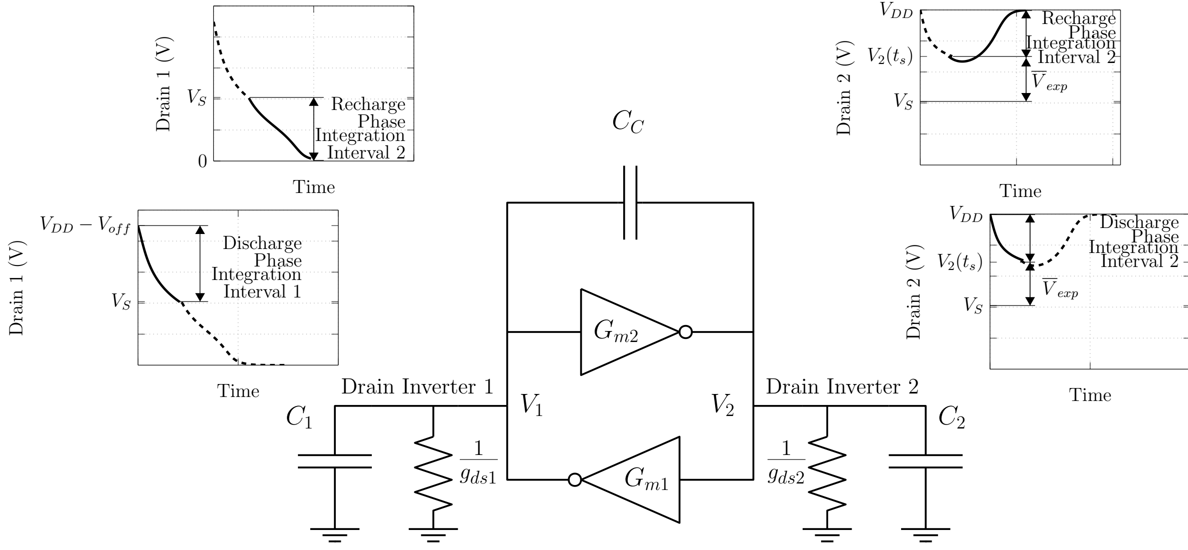


Figure 4.1: Illustration of the integration intervals in order to obtain a fixed value for the effective parameters.

of the loser inverter. Thus, the average integrals are given by

$$\overline{C}_{gsn1\alpha} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{V_2(t_s)}^{V_{DD}} \int_{V_S}^{V_{DD}-V_{off}} C_{gsn} dV_{gs} dV_{ds} \tag{4.7}$$

$$\overline{C}_{gsn1\beta} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{V_2(t_s)}^{V_{DD}} \int_{0}^{V_S} C_{gsn} dV_{gs} dV_{ds} \tag{4.8}$$

$$\overline{C}_{gsn2\alpha} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{V_S}^{V_{DD}-V_{off}} \int_{V_2(t_s)}^{V_{DD}} C_{gsn} dV_{gs} dV_{ds} \tag{4.9}$$

$$\overline{C}_{gsn2\beta} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{0}^{V_S} \int_{V_2(t_s)}^{V_{DD}} C_{gsn} dV_{gs} dV_{ds}. \tag{4.10}$$

Junctions and gate-to-body capacitances were considered to be bias independent, hence, (3.14) and (3.15) should provide $\overline{C}_{gb}$ and $\overline{C}_j$ straightforwardly.

Coupling capacitance can be decomposed into parasitics as in (3.4) Since coupling capacitance is composed only by transistor gate-to-drain capacitances, finding $C_C$ turns out to be very simple. We modeled $C_{gd}$ to be bias independent, so, $\overline{C}_{gd} = C_{gd}$ as defined in (3.13).

The effective capacitance for the $p$-type transistors can be obtained by switching and changing both integration limits in (4.7), (4.8), (4.9) and (4.10) by, respectively,

$$\overline{C}_{gsp1\alpha} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{0}^{V_{DD}-V_2(t_s)} \int_{V_{off}}^{V_{DD}-V_S} C_{gsp} dV_{gs} dV_{ds} \tag{4.11}$$

$$\overline{C}_{gsp1\beta} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{0}^{V_{DD}-V_2(t_s)} \int_{V_{DD}-V_S}^{V_{DD}} C_{gsp} dV_{gs} dV_{ds} \tag{4.12}$$

$$\overline{C}_{gsp2\alpha} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{V_{off}}^{V_{DD}-V_S} \int_{0}^{V_{DD}-V_2(t_s)} C_{gsp} dV_{gs} dV_{ds} \tag{4.13}$$

$$\overline{C}_{gsp2\beta} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{V_{DD}-V_S}^{V_{DD}} \int_{0}^{V_{DD}-V_2(t_s)} C_{gsp} dV_{gs} dV_{ds}. \tag{4.14}$$

**Transconductance**

The inverter transconductances, $G_{m1}$ and $G_{m2}$, are composed by the respectively $n$ and $p$-type transconductances, as defined in (2.7). In order to obtain constant values of $G_m$ for both discharging and regeneration phases, we take the average value of both transconductances for the intervals depicted in Fig. 4.1, the same way we approach the capacitances. The transconductances with subscripts 1 belong to inverter 1, transconductances with subscript 2 otherwise, so that we can obtain the integration intervals from Fig. 4.1 resulting in

$$\overline{G}_{mgn1\alpha} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{V_S}^{V_{DD}-V_{off}} \int_{V_2(t_s)}^{V_{DD}} G_{mgn} dV_{gs} dV_{ds} \tag{4.15}$$

$$\overline{G}_{mgn1\beta} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{0}^{V_S} \int_{V_2(t_s)}^{V_{DD}} G_{mgn} dV_{gs} dV_{ds} \tag{4.16}$$

$$\overline{G}_{mgn2\alpha} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{V_2(t_s)}^{V_{DD}} \int_{V_S}^{V_{DD}-V_{off}} G_{mgn} dV_{gs} dV_{ds} \tag{4.17}$$

$$\overline{G}_{mgn2\beta} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{V_2(t_s)}^{V_{DD}} \int_{0}^{V_S} G_{mgn} dV_{gs} dV_{ds}. \tag{4.18}$$

If the used parameters are the ones extracted by the MATLAB routine developed in this thesis, the integration intervals must be the same for both $n$ and $p$-type devices, because the schematic used for extraction already accounted for the $n$ to $p$-type terminal voltage changes, as showed in Fig. 4.2.

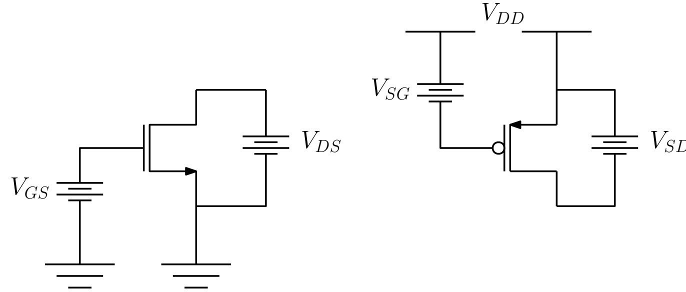


Figure 4.2: Schematic of the circuit for parameter extraction of transconductance and channel conductance.

### Channel Conductance

The inverter total channel conductances, $g_{ds1}$ and $g_{ds2}$, are composed by both inverter transistor channel conductances, as defined in (2.9) and (2.10).

The effective $g_{ds}$ values for the discharging and regeneration phases for both $n$ and $p$-type transistors can be obtained by applying the same integral with the same limits of (4.15), (4.16), (4.17) and (4.18), which results

$$\overline{g}_{dsn1\alpha} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{V_S}^{V_{DD}-V_{off}} \int_{V_2(t_s)}^{V_{DD}} g_{dsn} dV_{gs} dV_{ds} \tag{4.19}$$

$$\overline{g}_{dsn1\beta} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{0}^{V_S} \int_{V_2(t_s)}^{V_{DD}} g_{dsn} dV_{gs} dV_{ds} \tag{4.20}$$

$$\overline{g}_{dsn2\alpha} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{V_2(t_s)}^{V_{DD}} \int_{V_S}^{V_{DD}-V_{off}} g_{dsn} dV_{gs} dV_{ds} \tag{4.21}$$

$$\overline{g}_{dsn2\beta} = \frac{1}{\triangle V_{DS} \triangle V_{GS}} \int_{V_2(t_s)}^{V_{DD}} \int_{0}^{V_S} g_{dsn} dV_{gs} dV_{ds}. \tag{4.22}$$

In order to obtain the $p$-type effective values, the integration limits of (4.19), (4.20), (4.21) and (4.22) does not need to be switched or changed. For the same reason the integration limits of the effective transconductance integrations was not changed.

### Additional Simplifications

The set of equations derived for the latch time delay conflicts with the way we defined the effective parameters. Observe that one of the integration limits we used for each effective parameter in this section is bounded at $V_2(t_s)$. On the other hand, $V_2(t_s)$ in models 1, 2 and 3 is a function of $\overline{V}_{exp}$ given in (2.29), (2.41) and (2.53), whereas $\overline{V}_{exp}$ is a function of several effective parameters, (2.30), (2.42) and (2.54), which is conflicting. In order to avoid this situation we propose to simplify (2.30), (2.42) and (2.54) as

$$\overline{V}_{exp} = \left( \left( V_{indc} - V_S \right) \mathrm{e}^{\frac{1}{2}} + \frac{V_{off}}{2} \mathrm{e}^{\frac{1}{2}} \right) /2. \tag{4.23}$$

Such simplification strongly affects the delay models. We propose to compensate these simplifications by ignoring $g_{dsn}$ and $G_{mgp}$ in the discharging phase and ignoring $g_{dsp}$ and $G_{mgn}$ in the regeneration phase. In this way, the importance of the $n$-type transistor importance in the discharging phase is strongly accentuated, while the importance of the $p$-type transistor is accentuated during the regeneration phase. Such compensation will prove effective in Sec. 4.2.1, where simulations will show to

be in close agreement with the time delay models.

### 4.1.3 The Offset Voltage

The input offset voltage is a strong function of the latch transistor dimensions [8], while, $n$-type transistors might have a stronger influence if the input voltage levels are close to $V_{DD}$. Inversely, for the case of a $p$ tail latch (like the one mentioned in Sec. 2.1), where the input voltage level is nearly $GND$, the input offset voltages are mostly accounted by the latch $p$-type transistors [70–72].

Since our latch is designed to operate with input voltage levels close to $V_{DD}$, the latching $n$-type transistors are expected to have major influence in the input offset voltage. In [14] the contribution of the pass gates and the $p$-type transistors were neglected in the 7T-LTSA and only the $n$-type threshold voltages were considered in the input offset voltage. The resulting equation is given by

$$\sigma_{off} = \frac{\sqrt{2}\sigma_{V_{Tn}}}{1 - DCI - \lambda_n}, \tag{4.24}$$

where $\sigma_{off}$ is the desired input offset voltage standard deviation, $\lambda_n$ is the $n$-type DIBL effect, $\sigma_{V_{Tn}}$ is the $n$-type transistor threshold voltage standard deviation [8] and DCI is an effect called differential charge injection, which was not addressed in this study.

Although many simplifications were carried out in order to obtain (4.24), this equation is still accurate as long as the input voltage level is close to $V_{DD}$, not taking into account the DCI effect, since it does not influence the final result of this thesis.

## 4.2 Comparison with Simulations

### 4.2.1 Time Model

The right plot in Figs. 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9, 4.10 and 4.11 the simulations using the 7T-LTSA latch delay models derived in Sec. 2 given by (2.31), (2.43) and (2.55) are presented. The simulations were carried out for $L$=30 nm for all transistors, $V_{off}$=0.1$V_{DD}$ and $V_{DD}$=350 mV, 450 mV and 550 mV. The left plot in Figs. 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9, 4.10 and 4.11 the time delays obtained using Virtuoso for the same simulation aforementioned can be observed. In order to avoid strong charge injection effects, the 7T-LTSA tail transistor width was made equal to the sum of both $n$-type transistor widths.

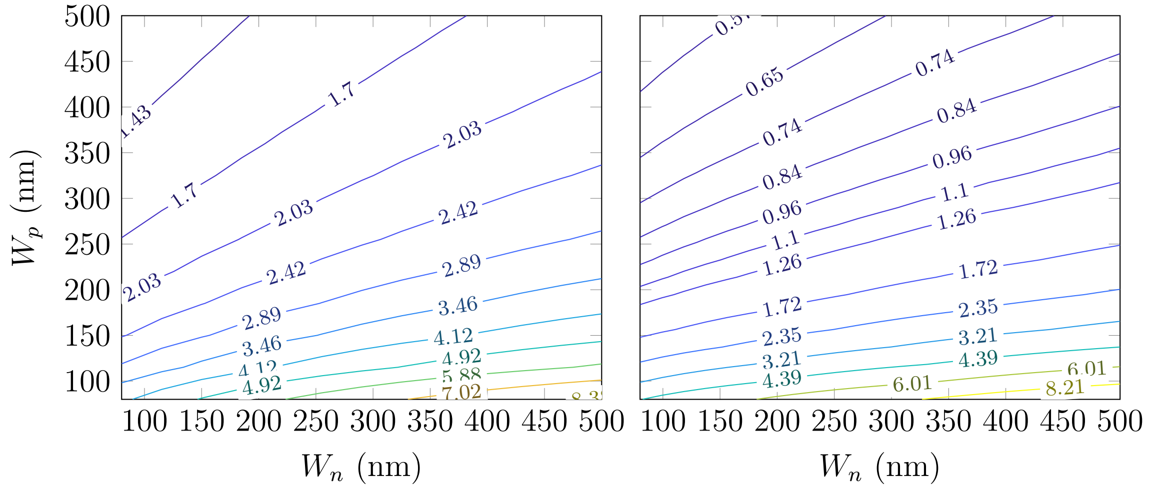


Figure 4.3: The simulated time delay (left) and obtained by using the time delay model given by (2.31) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=350 mV and $V_{off}$=35 mV (contour lines in nanoseconds).

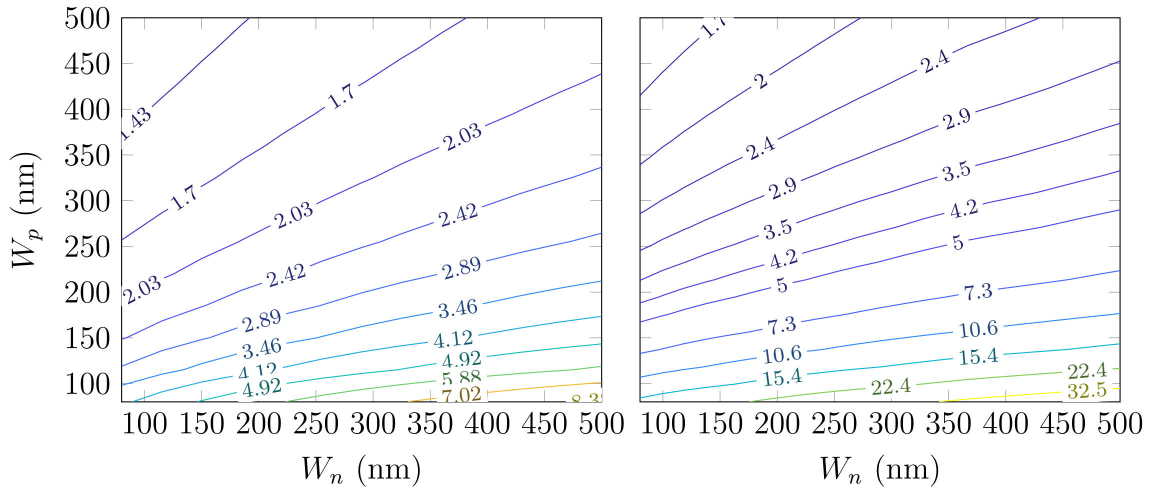


Figure 4.4: The simulated time delay (left) and obtained by using the time delay model given by (2.43) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=350 mV and $V_{off}$=35 mV (contour lines in nanoseconds).

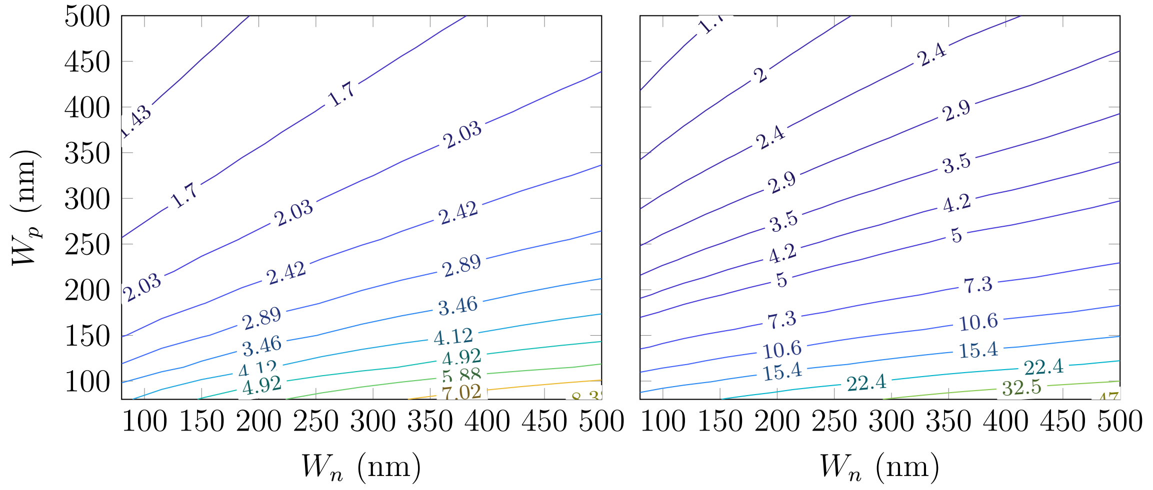


Figure 4.5: The simulated time delay (left) and obtained by using the time delay model given by (2.55) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=350 mV and $V_{off}$=35 mV (contour lines in nanoseconds).

Observe that Figs. 4.3, 4.3 and 4.3 indicated a non-trivial result. Unlike usual rule of thumb inverter design, the $p$ to $n$-type width ratio for constant length 3 to 1 is not the fastest solution for $V_{DD}$=350mV, the proposed models could predict that. On top of that, the surface of both simulation and time delay models were similar, which is the key factor for the latch design in Sec. 4.2.2.

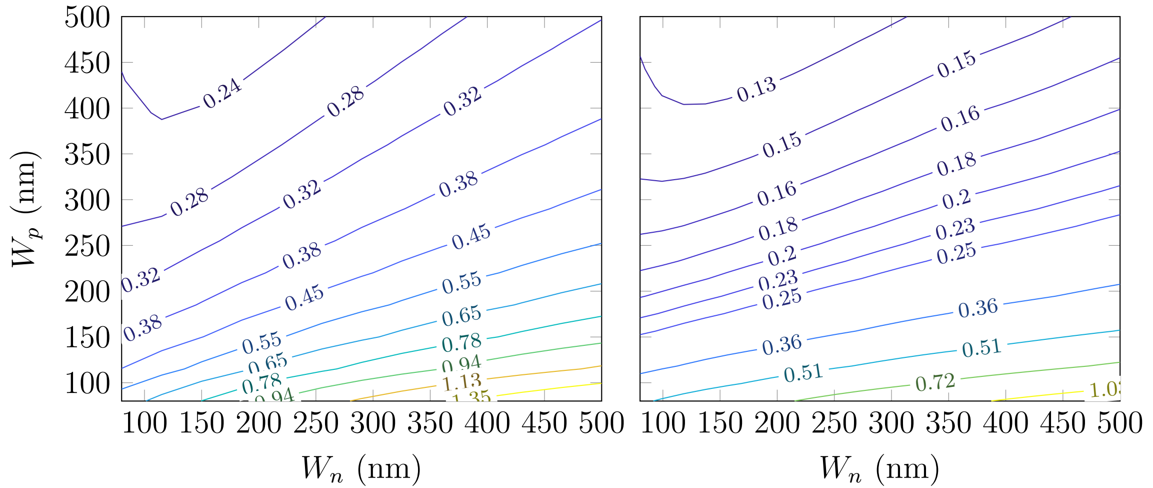


Figure 4.6: The simulated time delay (left) and obtained by using the time delay model given by (2.31) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=450 mV and $V_{off}$=45 mV (contour lines in nanoseconds).

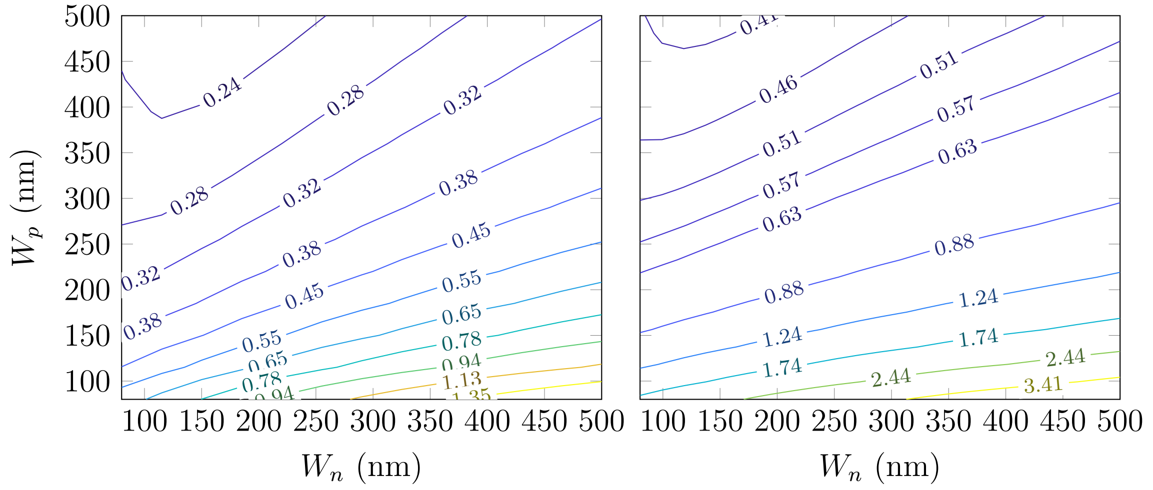


Figure 4.7: The simulated time delay (left) and obtained by using the time delay model given by (2.43) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=450 mV and $V_{off}$=45 mV (contour lines in nanoseconds).

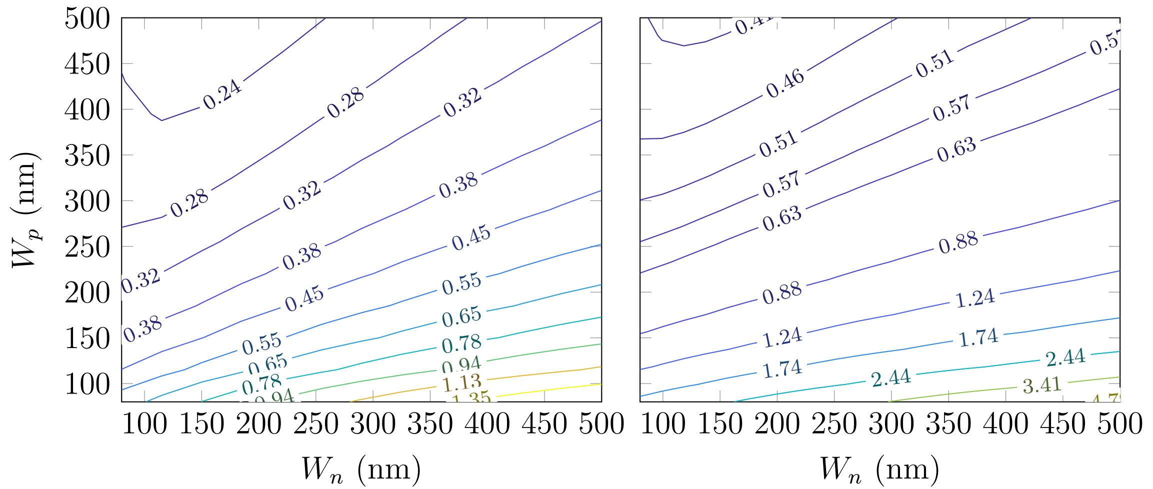


Figure 4.8: The simulated time delay (left) and obtained by using the time delay model given by (2.55) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=450 mV and $V_{off}$=45 mV (contour lines in nanoseconds).

In Figs. 4.6, 4.6 and 4.6 one can note that the minimum time delay is sliding towards the higher $W_n$ values.

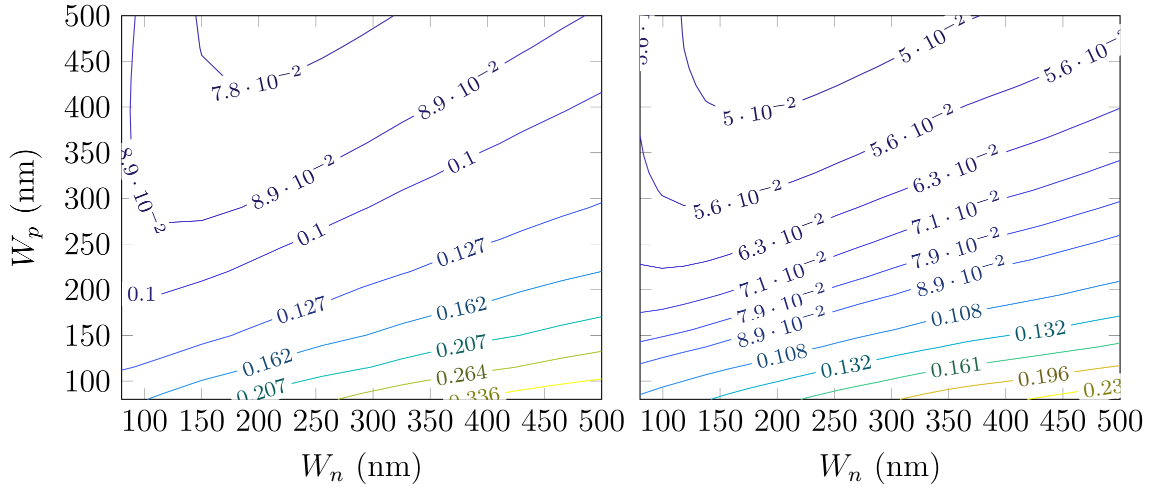


Figure 4.9: The simulated time delay (left) and obtained by using the time delay model given by (2.31) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=550 mV and $V_{off}$=55 mV (contour lines in nanoseconds).

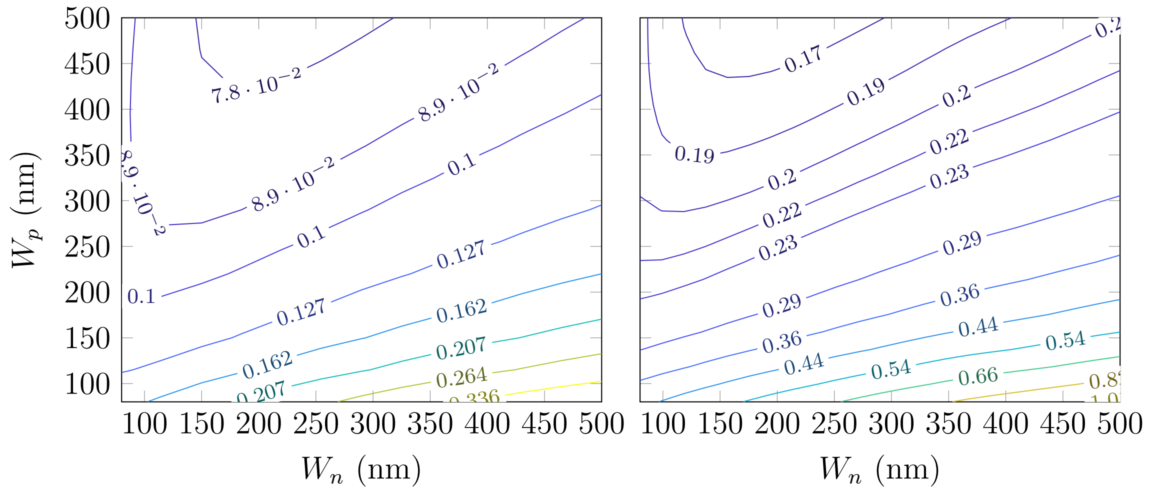


Figure 4.10: The simulated time delay (left) and obtained by using the time delay model given by (2.43) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=550 mV and $V_{off}$=55 mV (contour lines in nanoseconds).

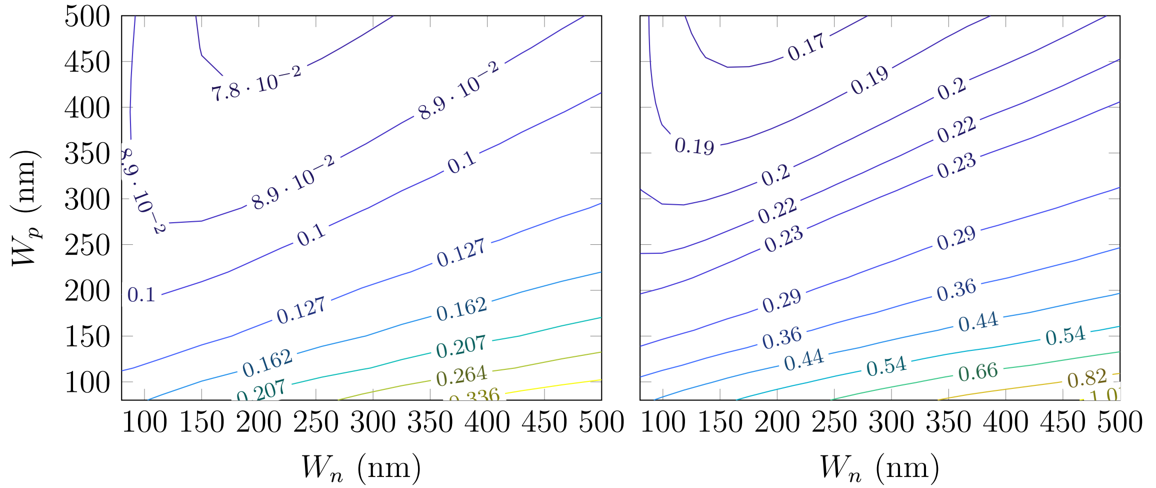


Figure 4.11: The simulated time delay (left) and obtained by using the time delay model given by (2.55) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=550 mV and $V_{off}$=55 mV (contour lines in nanoseconds).

Finally, in Figs. 4.3, 4.3 and 4.3 can be observed that the minimum time delay resides in a latch configuration with $p$ to $n$-type width ratio of 3, a well known result.

By visual inspection of Figs. 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9, 4.10 and 4.11 both simulations and models are in close agreement. It can be observed that the minimum time for every simulation sits at the design region boundary $W_p$=500 nm. It can also be observed that the $n$-type latching transistors become increasingly important as the $V_{DD}$ increases. Models (2.31), (2.43) and (2.55) were able to grasp this behavior. Tabs. 4.1, 4.2 and 4.3 show that models 1, 2 and 3, have similar minimum and maximum errors, contrary to initial expectations. This is justified by the several simplifications made in Sec. 4.1.2. Taking the average value of the small-signal parasitics is an oversimplification of the transistor behavior in a latch decision. Moreover, ignoring $g_{dsn}$ and $G_{mgp}$ in the discharging phase and $g_{dsp}$ and $G_{mgn}$ in the regeneration phase greatly closes the gap between simulations and all models, hence hiding the benefits of using (2.43) and (2.55) over (2.31).

Table 4.1: Mean and maximum errors between simulation and the proposed time delay models in Figs. 4.3, 4.4 and 4.5.

| 350 mV | Model 1 (2.31) | Model 2 (2.43) | Model 3 (2.55) |
|---|---|---|---|
| Mean Error (%) | 67.6 | 67.3 | 67.6 |
| Maximum Error (%) | 378.0 | 358.1 | 357.0 |

Table 4.2: Mean and maximum errors between simulation and the proposed time delay models in Figs. 4.6, 4.7 and 4.8.

| 450 mV | Model 1 (2.31) | Model 2 (2.43) | Model 3 (2.55) |
|---|---|---|---|
| Mean Error (%) | 75.9 | 74.9 | 74.9 |
| Maximum Error (%) | 434.0 | 442.0 | 442.1 |

Table 4.3: Mean and maximum errors between simulation and the proposed time delay models in Figs. 4.9, 4.10 and 4.11.

| 550 mV | Model 1 (2.31) | Model 2 (2.43) | Model 3 (2.55) |
|---|---|---|---|
| Mean Error (%) | 57.0 | 58.2 | 58.3 |
| Maximum Error (%) | 289.8 | 304.0 | 304.8 |

The minimum simulated time delay value for each supply voltage level can be found in Tab. 4.4. The respective latching transistors widths can be found in Tab. 4.5. Model 1 usually produces an optimistic estimation of the latch delay, whereas Models 2 and 3 presents much higher delay values. Both are nearly equidistant from the simulated minimum time delay, which is the reason why Tabs. 4.1, 4.2 and 4.3 show similar errors, while from Tab. 4.4 it is evident that the addition of coupling capacitances significantly slows the 7T-LTSA transient decision. On the other hand, $g_{ds}$ has very little effect. The latching transistor sizes for each minimum time delay were roughly equal to those of Models 1, 2 and 3. Moreover, although minimum time delay obtained by the proposed models were just close to the reference results, the corresponding latching transistor sizes were the same for $V_{DD}$=550 mV and quite close for $V_{DD}$=350 mV and and $V_{DD}$=450 mV, where weak and moderate inversion are dominant.

Table 4.4: Minimum time delay value obtained by simulation and the proposed models.

| $V_{DD}$ | Simulated | Model 1 (2.31) | Model 2 (2.43) | Model 3 (2.55) |
|---|---|---|---|---|
| 350 mV | 1.3 ns | 510 ps | 1.5 ns | 1.5 ns |
| 450 mV | 227 ps | 120 ps | 397 ps | 399 ps |
| 550 mV | 76 ps | 46 ps | 164 ps | 165 ps |

Table 4.5: Latching $n$-type width at the minimum time delay for both simulations and time delay models. The $p$-type width obtained was 500 nm in either simulations and time delay models.

| $V_{DD}$ | Simulated | Model 1 (2.31) | Model 2 (2.43) | Model 3 (2.55) |
|---|---|---|---|---|
| 350 mV | $W_n$=85 nm | $W_n$=115 nm | $W_n$=115 nm | $W_n$=115 nm |
| 450 mV | $W_n$=155 nm | $W_n$=190 nm | $W_n$=190 nm | $W_n$=190 nm |
| 550 mV | $W_n$=220 nm | $W_n$=220 nm | $W_n$=220 nm | $W_n$=220 nm |

### 4.2.2 Cost Function

The left plot in Figs. 4.12, 4.13 ,4.14, 4.15, 4.16 ,4.17, 4.18, 4.19 and 4.20 the evaluation of (4.2) obtained using Virtuoso are presented. The simulations consist of 507 latch configurations by varying $W_n$ and $W_p$ from 80 nm to 500 nm in 13 steps each, for $V_{DD}$=350 mV, $V_{DD}$=450 mV and $V_{DD}$=550 mV, $\Delta V_{in}$ fixed at $0.1V_{DD}$, and $L$=30 nm. A monte carlo simulation with 500 runs was carried out for each latch configuration. The simulations were carried out using 10 desktops using 8 cores at 4 GHz and 32 GB of RAM, taking 28 hours for completion.

The plot on the right in Figs. 4.12, 4.13 ,4.14, 4.15, 4.16 ,4.17, 4.18, 4.19 and 4.20 were generated through MATLAB routines using (2.31), (2.43) and (2.55) for the time delay models and (4.24) and (1.3) for the yield model. The simulations consisted of 1087 latch configurations for each time delay model by varying $W_n$ and $W_p$ from 80 nm to 500 nm with 23 steps each for supply voltages of 350 mV, 450 mV and 550 mV. For fair comparison, the fixed parameters were the same as the ones used to generate the left plot in Figs. 4.12, 4.13 ,4.14, 4.15, 4.16 ,4.17, 4.18, 4.19 and 4.20. The MATLAB routine was executed using a notebook with 8 GB of RAM and 4 dedicated cores with 4 GHz each. The simulations took 2 hours for the 3 models. Even thought the reference simulations had more computational power, the MATLAB routine using the proposed models more than outmatched the Virtuoso simulations in terms of speed.

Comparing both the left and right plots Figs. 4.12, 4.13 ,4.14, 4.15, 4.16 ,4.17, 4.18, 4.19 and 4.20 we conclude that the models are rather effective. Tabs. 4.6, 4.7 and 4.8 present the mean and maximum errors, and the yield values are in Tab 4.9. Observe that the yield obtained using (4.24) and (1.3) is more pessimistic than the one obtained through simulations, which does not affect the cost function surface, and consequently, the optimum value position.

If very stringent yield requirement are needed, one can use

$$FOM = \frac{Y(W,L)^{\kappa}}{t_d(W,L)/t_{min}} \tag{4.25}$$

instead of (4.2), where $\kappa$ is the weighting factor. For $\kappa$ higher than 1, yield ($Y(W, L)$) below 100 % tends to be heavily punished, and (4.25) will displace the maximum of the cost function toward bigger $W_n$ values.

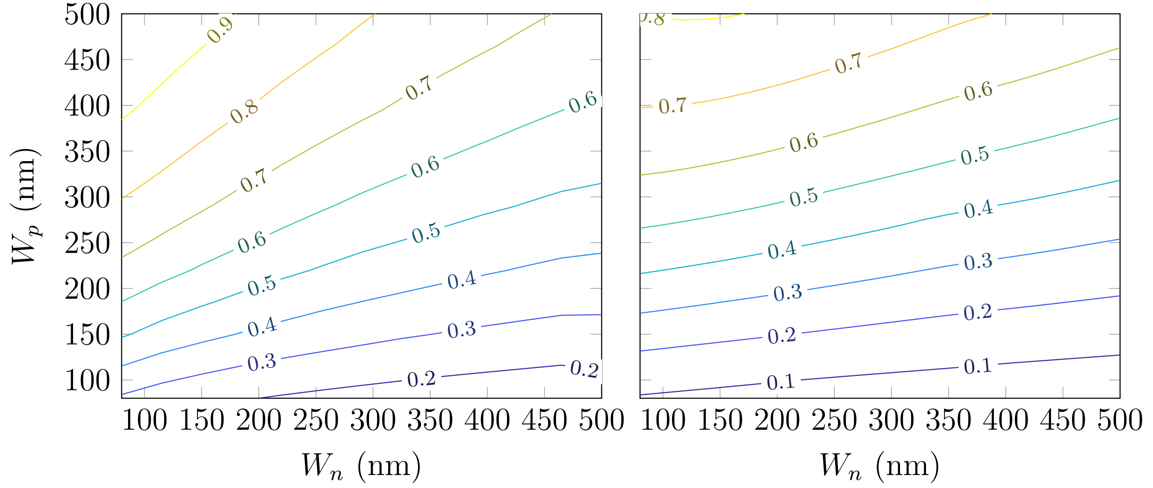


Figure 4.12: The simulated (4.2) (left) and obtained by using the time delay model given by (2.31) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=350 mV and $V_{off}$=35 mV.

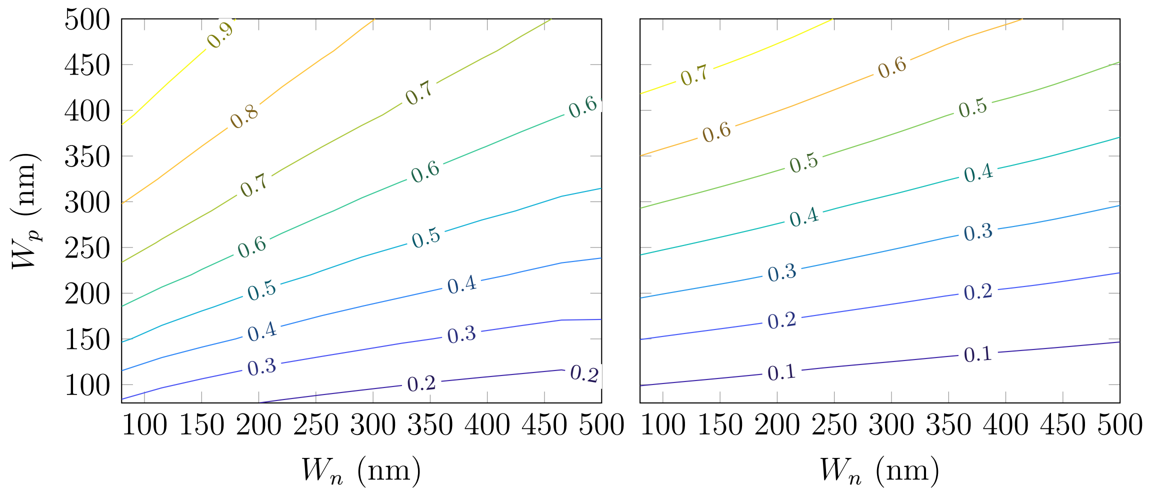


Figure 4.13: The simulated (4.2) (left) and obtained by using the time delay model given by (2.43) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=350 mV and $V_{off}$=35 mV.

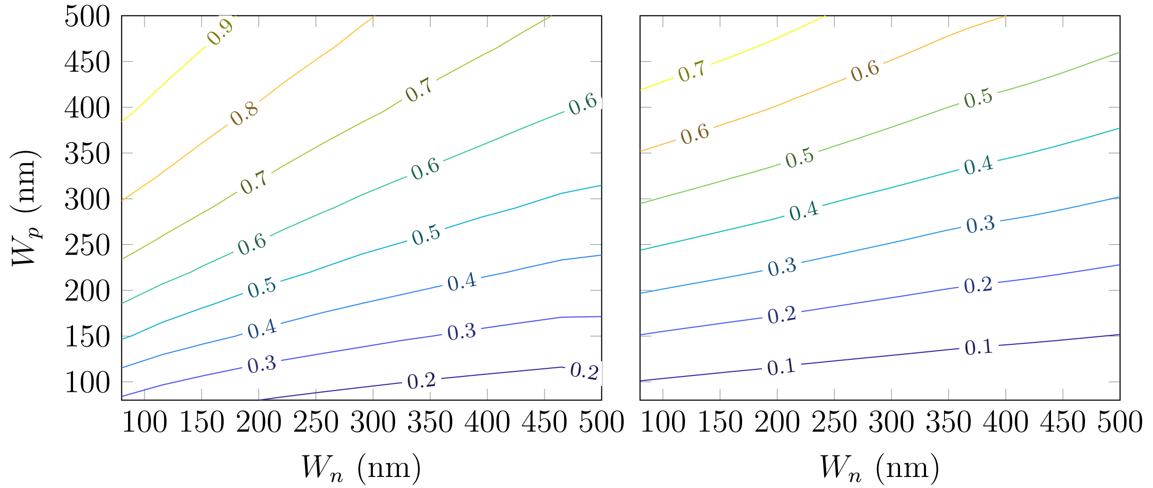


Figure 4.14: The simulated (4.2) (left) and obtained by using the time delay model given by (2.55) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=350 mV and $V_{off}$=35 mV.

Because the surfaces of both simulations and time delay models in Figs. 4.3, 4.3 and 4.3 are similar, the surfaces of Figs. 4.12, 4.13 and 4.14 are similar as well, allowing the designer to select the best latch in terms of the compromise defined by (4.2).

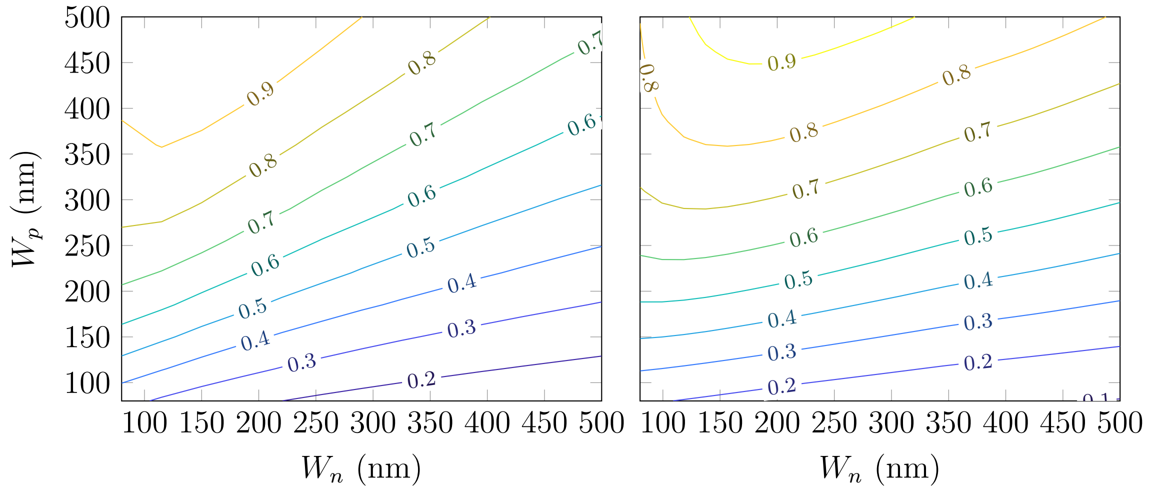


Figure 4.15: The simulated (4.2) (left) and obtained by using the time delay model given by (2.31) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=450 mV and $V_{off}$=45 mV.

Near-threshold circuit operation is historically very complicated to study [21]. Nevertheless, the surfaces obtained from simulations and by models proposed in this thesis are close, even though the small-signal parameters evaluated in Chapter. 3 had significant mean and maximum errors. Allowing the designer to use (4.2) for latch design even for $V_{DD}$ close to the threshold voltage value.

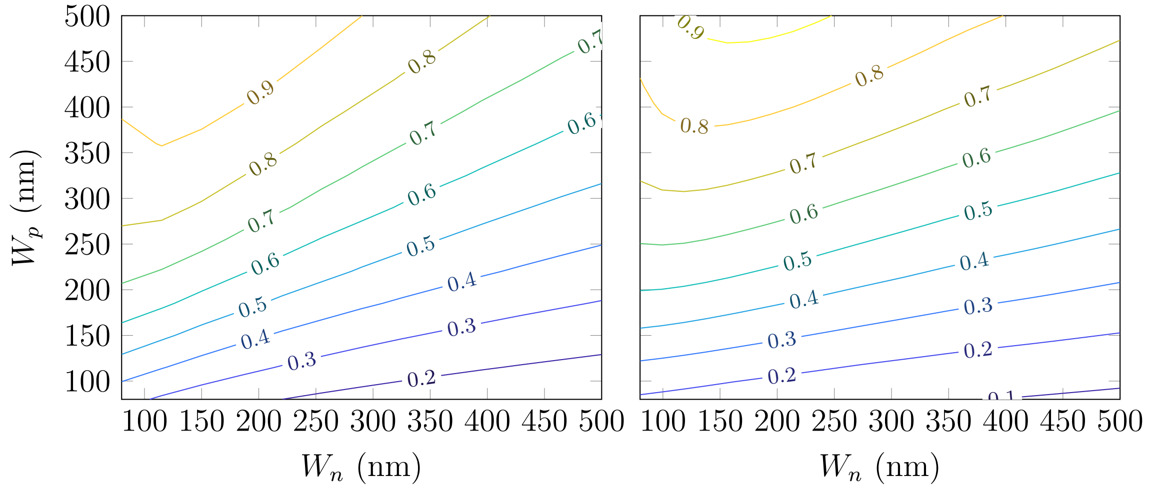


Figure 4.16: The simulated (4.2) (left) and obtained by using the time delay model given by (2.43) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=450 mV and $V_{off}$=45 mV.

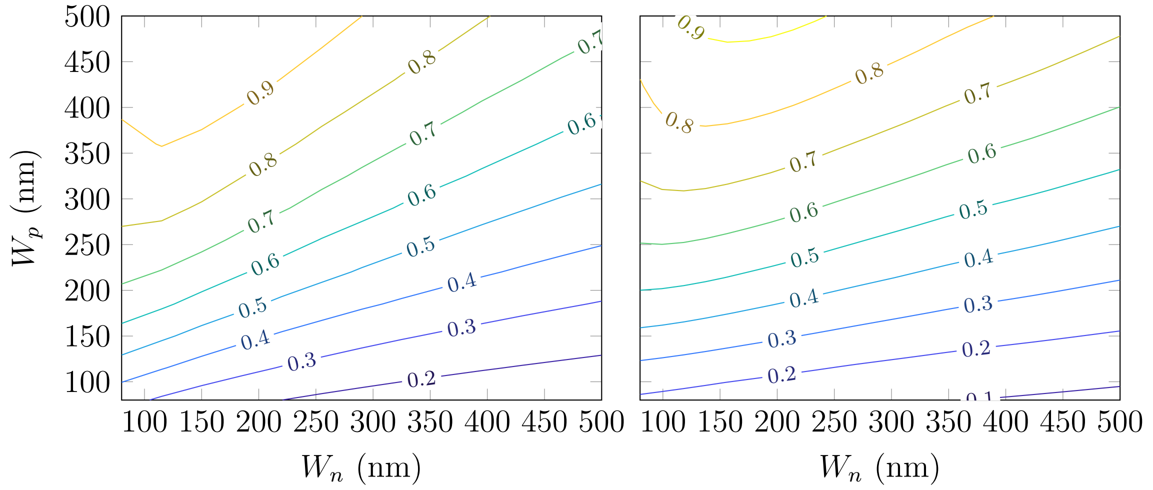


Figure 4.17: The simulated (4.2) (left) and obtained by using the time delay model given by (2.55) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=450 mV and $V_{off}$=45 mV.

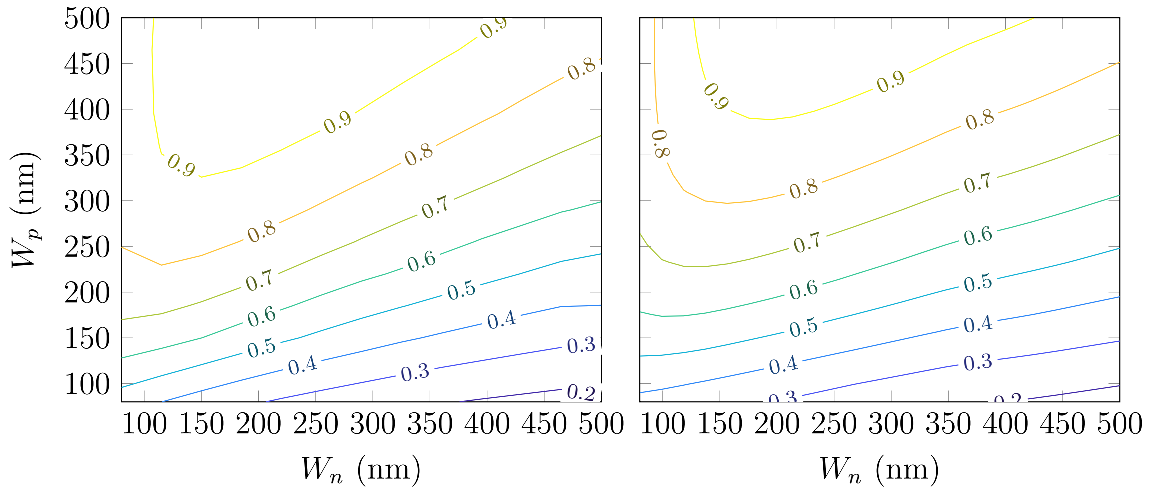


Figure 4.18: The simulated (4.2) (left) and obtained by using the time delay model given by (2.31) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=550 mV and $V_{off}$=55 mV.

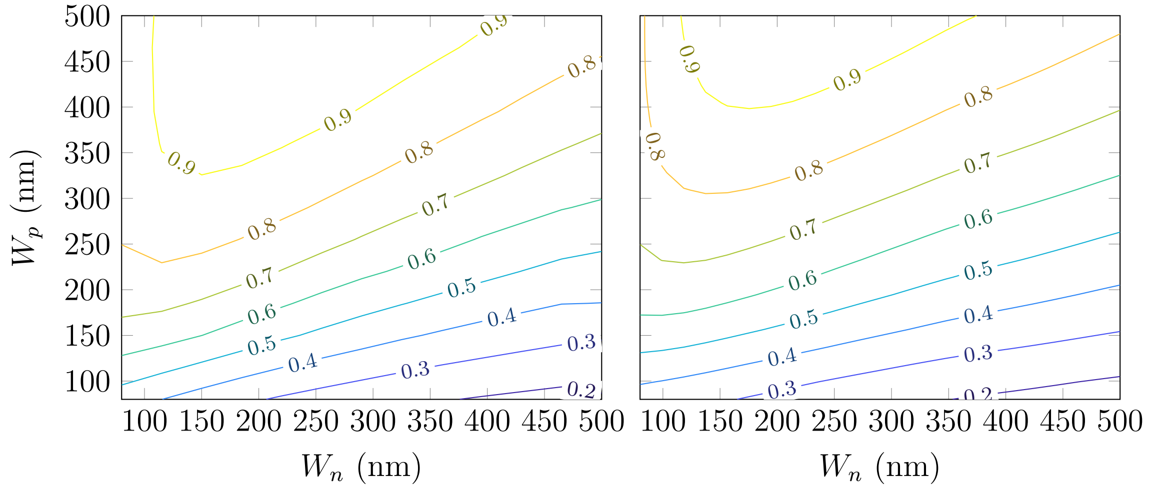


Figure 4.19: The simulated (4.2) (left) and obtained by using the time delay model given by (2.43) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=550 mV and $V_{off}$=55 mV.

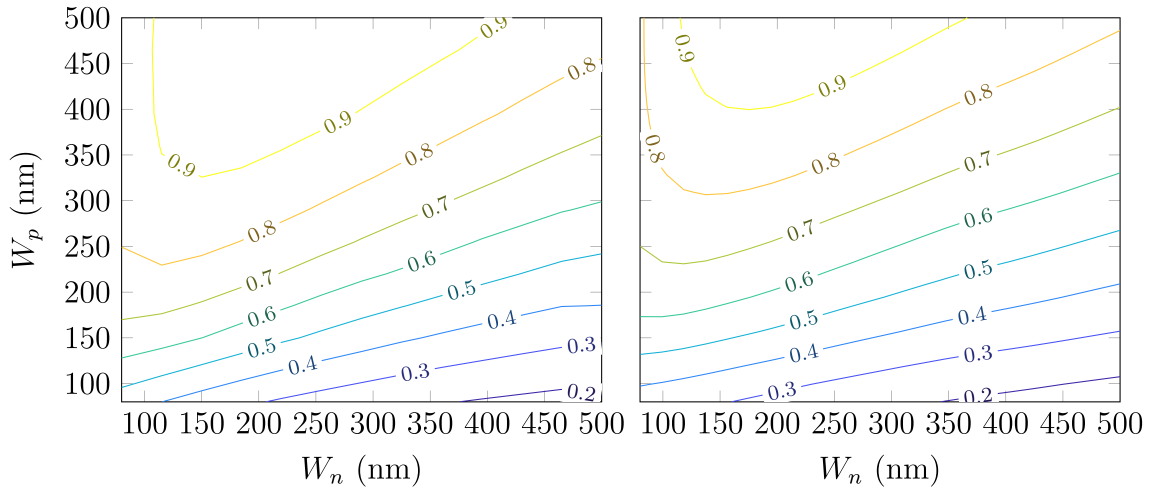


Figure 4.20: The simulated (4.2) (left) and obtained by using the time delay model given by (2.55) (right) varying $n$ and $p$-type widths for fixed $L$=30 nm for the latching transistors, $V_{DD}$=550 mV and $V_{off}$=55 mV.

Because of the minimum time delay slide observed in Sec. 4.2.1 due to the $V_{DD}$ increase, the surface obtained by simulation observed in Figs. 4.18, 4.19 and 4.20 slides as well. It can also be observed that the proposed approach could predict such behavior.

Table 4.6: Mean and maximum errors between simulation and the proposed models in Figs. 4.12, 4.13 and 4.14.

| $V_{DD}$=350 mV | (4.2) using Model 1 | (4.2) using Model 2 | (4.2) using Model 3 |
|---|---|---|---|
| Mean Error (%) | 29.3 | 39.7 | 41.0 |
| Maximum Error (%) | 69.3 | 76.6 | 79.3 |

Table 4.7: Mean and maximum errors between simulation and the proposed models in Figs. 4.15, 4.16 and 4.17.

| $V_{DD}$=450 mV | (4.2) using Model 1 | (4.2) using Model 2 | (4.2) using Model 3 |
|---|---|---|---|
| Mean Error (%) | 9.8 | 14.3 | 15.1 |
| Maximum Error (%) | 38.3 | 45.3 | 46.1 |

Table 4.8: Mean and maximum errors between simulation and the proposed models in Figs. 4.18, 4.19 and 4.20.

| $V_{DD}$=550 mV | (4.2) using Model 1 | (4.2) using Model 2 | (4.2) using Model 3 |
|---|---|---|---|
| Mean Error (%) | 5.0 | 7.5 | 8.3 |
| Maximum Error (%) | 17.9 | 20.4 | 20.9 |

Table 4.9: Yield obtained through simulation and using (4.24) and (1.3) at the maximum cost function value.

| $V_{DD}$ | Simulated | (4.24) and (1.3) |
|---|---|---|
| 350 mV | 99.6 % | 85.3 % |
| 450 mV | 99.8 % | 95.3 % |
| 550 mV | 100.0 % | 98.8 % |

## 4.3 Comparisons With Other Works

The proposed 7T-LTSA is the most basic latch structure which is well known for a couple of decades. Several other latch architectures can outrun the 7T-LTSA in speed, yield, energy consumption or all three performance parameters together. With the advance of technology, faster, robust and efficient transistors have taken place allowing classical circuit architectures to achieve impressive performance, much better than any other circuit from previous processes. We illustrate the properties in Figs. 4.21, where speed and delay are compared with some works in the recent year. It is clear that the 7T-LTSA with the proposed optimization using the 28 nm UTBB FDSOI CMOS process have comparable performance even with a much lower supply voltage level. In Tab. 4.10 the process and supply voltage value of the works compared with the proposed latch are presented.

Several other works provide data exclusively on offset or speed and cannot be

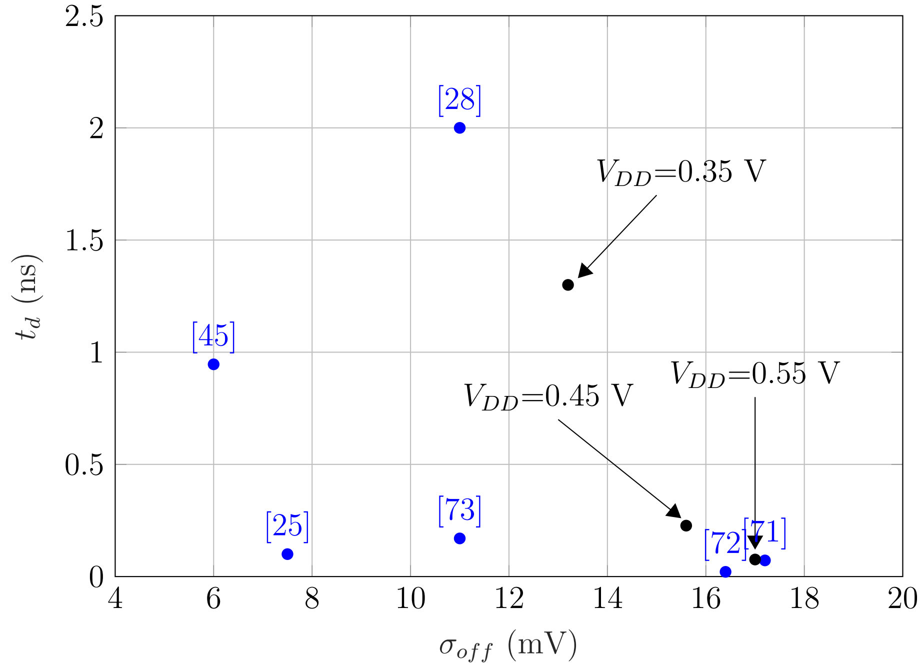


Figure 4.21: Comparison of the proposed 7T-LTSA optimized using (4.2) with some recent works.

Table 4.10: Latches supply voltage levels and process for the works in Fig. 4.21.

| Work | Process | Supply Voltage Level |
|---|---|---|
| [45] | 65 nm CMOS | 1.2 V |
| [28] | 65 nm GP CMOS | 0.5 V |
| [25] | 65 nm CMOS | 0.6 V |
| [72] | 90 nm CMOS | 1 V |
| [73] | 28 nm CMOS | 1 V |
| [71] | 180 nm CMOS | 1.8 V |

used for fair comparison in Fig. 4.21. Among such studies, we cite some of then in order to strengthen the argument that the proposed optimization procedure using a state-of-art process leads to great performance 7T-LTSAs. Work [74] uses a 13T sense amplifier architecture in a 45 nm CMOS process with a delay of 58.6 ps at 0.6 V and 243.3 ps at 0.4 V, which is comparable with the performances obtained in this thesis. In [75] a comparative study of conventional latches is advanced. The fact that the $n$ type latching transistors strongly affects the latch offset is mentioned, and input voltage offset is mitigated by resizing the pull-down transistors. For fair comparison with the proposed 7T-LTSA, we picked data corresponding for $n$-type latching transistors with aspect ratio equal to 8. The source coupled latch architecture had a $\sigma_{off}$=40 mV, the schmitt trigger sense amp architecture had $\sigma_{off}$=23 mV, the 2-stack transistor latch had $\sigma_{off}$=27 mV and the 3-stack transistor latch had $\sigma_{off}$=30 mV. These values were obtained at $V_{DD}$=1 V with a 45 nm

CMOS process. From 4.21 it is clear that the proposed latches have low $\sigma_{off}$ for every simulated supply voltage levels.

Of course, the works presented in this section were selected to advocate this research. Several other latches can outrun the latch designed in this work, specially the latches manufactured with more sophisticated processes, some of then can be found in [76] where several architectures have even lower $\sigma_{off}$ than found in this thesis, however, it is clear that the procedure developed in this thesis produces good results for the classical latch. It should be observed that the approach used in this thesis can be applied to other latches as well. The double-tail latch can be optimized by noting that $\sigma_{off}$ is strongly mitigated by proper sizing of the tail differential pair, and by modeling the tail transistors as current sinks and adding the tail transistor junction capacitance to the output node.

## 4.4 Summary

In this chapter we evaluated the time delay models developed in Chapter 2. Small-signal models derived in Chapter 3 were needed in order to link transistor width and length with latch time delay. Several simplifications were applied in order to obtain a compact set of equations which could grasp the simulated delay values inside the design region defined in Sec. 3.1.3. The aforementioned simplifications paid off since the models showed close agreement with simulations, as observed comparing Figs. 4.3, 4.4, 4.5, 4.6, 4.7, 4.8, 4.9, 4.10 and 4.11. Tabs. 4.1, 4.1 and 4.1 also show close agreement between models and simulations, whereas, Tabs. 4.4 and 4.5 gave more interesting results, which are good approximations of the minimum latch decision time delay value and the position inside the design region.

A cost function used for latch optimization was introduced as well. The models for $\sigma_{off}$, $V_S$ and $t_d$ allowed the analytical 7T-LTSA design in terms of speed and yield. The models showed close agreement with simulations as can be verified in Figs. 4.12, 4.13 ,4.14, 4.15, 4.16, 4.17, 4.18, 4.19 and 4.20. One of the main contributions of this thesis is the reduced computational effort needed to evaluate (4.2) with the proposed models instead of by simulations. In Sec. 4.3 we compared the performance of some latches found in recent works with the proposed latch. Using the approach developed in this thesis with the 28 nm UTBB FDSOI CMOS process led to a 7T-LTSA with comparable or better performance than some fancy latch architectures using older processes.

It is important to note that the optimum latch found in this thesis is obtained by using (4.2) as a cost function. However, this does not mean that (4.2) leads to the best latch for every application. Robust latch design requires extremely low $\sigma_{off}$, and therefore the proposed cost function might lead to a latch configuration

which does not comply with the application. Moreover the compromise between yield and speed could be adjusted by using (4.25) by setting $\kappa$ properly. For the latch optimization, it is up to the designer to judge which parameter should be targeted.

# Chapter 5

# Conclusion

This thesis focused in the design of a 7T-LTSA for operating in a wide supply voltage range. The development of time delay equations is the major contribution of this work since, to the best of our knowledge, near-threshold operations time analysis for the latch transient response is not reported yet. Analysis of the small-signal parameters under severe short-channel effects for sub/near-threshold operations were necessary. Finally, we proposed a cost function which was used to find the best latch configuration in terms of speed and yield for a given voltage supply level and input differential voltage. This chapter summarizes the contributions of this thesis and discusses the future directions.

## 5.1 Time Delay Models

In Chapter 2 we approached the latch transient behavior by mathematical means, not caring much about small-signal properties of the transistor. This proved to be a much more promising approach than developing differential equations by using complex transconductance models such as (3.26). Several simplifications for classical transconductance equations were applied, whereas no simplification led to a closed form solution. The complex transistor dynamic characteristics were concentrated in the effective parameters and treated in Chapters 3 and 4.

The core of the thesis is the concept of metastability voltage, since, by using such concept, we derived a small-signal circuit for the 7T-LTSA, proposed several time delay models, abandoned the obsolete latch decision events mentioned in Sec. 2.1, and defined a threshold independent description. All proposed time delay models are in close agreement with simulations. Surprisingly, the model which best predicted the simulated results was the least complex one.

Computational effort was also a concern. Evaluating time delay by using (2.31), the other needed equations provided in Chapters 2 and 4 and the fitted parameters extracted in Chapter 3 showed to be more time efficient than using sophisticated

simulators such as Virtuoso. In fact, as mentioned in Sec. 4.2.2, evaluating (4.2) using the proposed equation was 14 times faster for a grid of latch configurations four times bigger even with less computational power, as mentioned in Chapter 4.

## 5.2 Small-Signal Parameter Analysis

As mentioned in Sec. 5.1, the time delay models simplify the transistor behavior, and hence extra complexity was needed in order to bring effects related to short-channel and limited voltage supply to our model. We proposed to approach such effects by analyzing and modeling small-signal parameter behavior inside a design region defined by the range of values where bias voltages, transistor length and width can vary. Several small-signal capacitances, transconductances and channel conductances for both $n$ and $p$-type transistors from the 28 nm UTBB FDSOI CMOS process were studied and modeled. Several fitting parameters were extracted. Mean and maximum errors between simulations and models for the design region corners were provided. Every model showed close agreement with simulations.

Among the models provided, we point out some which had a remarkably performance. The $C_{gs}$ model on top of being highly accurate (worst case mean error below 7.5 %), is far less complex than charge based models small-signal capacitance. The assumption of breaking $C_{gs}$ into intrinsic and extrinsic parts is justified by the nearly constant fitting parameter $C'_{gs_{extrinsic}}$ obtained for every simulation. The $G_m$ model had higher mean and maximum errors, whereas the addition of a single parameter to the classical transconductance equation already improves $G_m$ predictability significantly. Both equations shall be improved and published in the future.

## 5.3 Cost Function and Optimum Latch

In Sec. ?? the proposed cost function was introduced. It is based on the figure of merit proposed by [1], which is maximized when yield is maximum and time delay is minimum. The aforementioned features and their simplicity are the motivations behind using it as a cost function. The final result is non-trivial. We found out that the $n$-type latching transistors are the most important ones, since larger $n$-type transistors significantly improve yield (for high input common mode voltage) and reduce latch discharging time. The $p$-type transistors have little effect in yield because the bitlines are discharged from $V_{DD}$.

Computational effort is improved. The simulation carried out using the proposed approach showed to be several times faster than by using Virtuoso. As mentioned in Chapter 4, even if using much more computational power, the proposed approach produced similar results in lower time.

## 5.4 Future Directions

The gap between sub/near-threshold operations and latch speed and yield characterization was filled by this research. This work can be used for digital circuit design for extreme low voltage application. The chip should be sent to manufacture in order to validate the developed tools, which can be used to provide the best latch configuration in terms of speed and yield.

Latch performance can be improved by other architectures as mentioned in Sec. 4.3, and the research advanced in this work can push the state-of-art line if applied in more sophisticated process. In fact, companies such as Samsung[1] and TSMC[2] are pushing digital circuit evolution by developing smaller FinFET processes, and hence polishing classical architectures can still find room in nowadays circuits.

Performance is not the only thread of improvement for this thesis. Computational effort was a major concern. Although improvement was accomplished, better models for the effective parameters can improve cost function evaluation speed. The integrals carried out in Sec. 4.1.2 are the most time consuming operations in the algorithm, and therefore should be avoided so that cost function evaluation time could be improved.

[1]https://www.samsung.com/semiconductor/
[2]https://www.tsmc.com/

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