DIGITAL ONE-CYCLE CONTROL TECHNIQUE WITH GRID VOLTAGE MEASUREMENT APPLIED TO THREE-PHASE POWER FACTOR CORRECTED RECTIFIERS AND ACTIVE POWER FILTERS

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Dissertação de Mestrado apresentada ao Programa de Pós-graduação em Engenharia Elétrica, COPPE, da Universidade Federal do Rio de Janeiro, como parte dos requisitos necessários à obtenção do título de Mestre em Engenharia Elétrica.

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with me, Guiding me.

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To doubt everything and to believe everything are two equally convenient solutions; each saves us from thinking.

— Jules Henri Poincaré (1854 - 1912)

Resumo da Dissertação apresentada à COPPE/UFRJ como parte dos requisitos necessários para a obtenção do grau de Mestre em Ciências (M.Sc.)

TÉCNICA DE CONTROLE POR UM CICLO DIGITAL COM MEDIÇÕES DE TENSÃO DE REDE APLICADA A RETIFICADORES FATOR DE POTÊNCIA CONTROLADO E FILTROS ATIVOS DE POTÊNCIA TRIFÁSICOS

Armando José Gomes Abrantes Ferreira

Março/2019

Orientadores: Luís Guilherme Barbosa Rolim
Robson Francisco da Silva Dias

Programa: Engenharia Elétrica

Considerando a demanda por melhorias nas cargas elétricas domésticas e industriais para atender às metas desafiadoras de satisfazer a demanda cada vez maior de energia elétrica e reduzir as emissões de gases de efeito estufa, o presente trabalho visa aplicar o Controle de Um Ciclo Digital (DOCC) com medição de tensão de rede para retificadores de fator de potência corrigida (PFC) e filtro ativo de potência (APF) trifásicos. O uso de tensão de rede é explorado em uma abordagem generalizada, definindo a influência dessas medições nas taxas de distorção harmônicas, fator de potência e limites de operação de carga. A compensação de queda de tensão indutiva e o uso de PWM Híbrido também são aplicados para melhorar o fator de potência e o uso do barramento CC. Resultados de simulação e experimentais da técnica OCC Digital aplicada a retificadores PFC e APF são apresentados, analisados e comparados com resultados experimentais e de simulação de técnicas convencionais para cada sistema.

Abstract of Dissertation presented to COPPE/UFRJ as a partial fulfillment of the requirements for the degree of Master of Science (M.Sc.)

DIGITAL ONE-CYCLE CONTROL TECHNIQUE WITH GRID VOLTAGE MEASUREMENT APPLIED TO THREE-PHASE POWER FACTOR CORRECTED RECTIFIERS AND ACTIVE POWER FILTERS

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March/2019

Advisors: Luís Guilherme Barbosa Rolim
Robson Francisco da Silva Dias

Department: Electrical Engineering

Considering the demand for improvements on domestic and industrial electrical loads to meet challenging goals of keeping up to an ever increasing demand of electrical energy and on the reduction of greenhouse gas emissions, the present work aims to apply the Digital One Cycle Control (DOCC) with grid voltage measurement to three-phase Power Corrected (PFC) Rectifier and Active Power Filter (APF). The use of grid voltage is explored in a generalized approach, by defining the influence of these measurements on harmonics, power factor and load limits. The compensation of inductive voltage drop and the use of Hybrid PWM are also applied to improve the power factor and the DC bus usage. Simulation and experimental results of the OCC digital technique applied to PFC and APF rectifiers are presented, analyzed and compared to simulation and experimental results of conventional technique for each system.

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List of Abbreviations

APF	Active Power Filters, p. 3
BEBS	Balanced Energy Based Schemes for Control of APF, p. 18
CBPWM	Carrier-Based PWM Modulation, p. 45
CCM	Continuous Conduction-Mode, p. 28
DOCC	Digital One-Cycle Control, p. 4
FOCC	Fast Response One-Cycle Control, p. 4
GCI	Grid Connected Inverter, p. 4
HEBS	Harmonic Extractor-Based Strategies for Control of APF, p. 17
HPWM	Hybrid PWM Modulation, p. 45
NLC	Non-Linear Carrier, p. 29
OCC	One Cycle Control, p. 3
PCC	Point of Common Coupling, p. 1
PF	Power Factor, p. 3
PLL	Phase-Lock-Loop, p. 6
PLL	Phase-Locked Loops, p. 10
PWM	Pulse Width Modulation, p. 3
SVPWM	Space Vector PWM Modulation, p. 45
THD	Total Harmonic Distortion, p. 5
d	Duty-Cycle, p. 24

List of Symbols

I_g^*	Grid Current Reference Amplitude, p. 3
L_g	Converter Inductance, p. 12
R_{DC}	DC-bus Voltage Regulator, p. 3
R_{es}	Modified Emulated Resistance, p. 66
R_{ig}	Current Regulator, p. 3
T_s	Switching Period, p. 24
V_m	Output of DC-bus Regulator in One-Cycle-Control, p. 3
V_o	Converter Output Voltage, p. 29
V_{N0}	Common-Mode Voltage, p. 11
V_{ms}	Modified Output of DC-bus Voltage Regulator, p. 36
X_s	Amplitude of Space Vector of Generic Variable, p. 11
$\bar{p}$	Average Part of Instantaneous Active Power, p. 20
$\bar{q}$	Average Part of Instantaneous Imaginary Power, p. 20
λ	Duty Cycle Convergence Ratio of Poincaré Maps, p. 56
$\mathbf{I}_{dq}$	Vector of Converter Pole Voltages in dq-Reference Frame in Frequency Domain, p. 12
$\mathbf{I}_{dq}$	Vector of Grid Currents in dq-Reference Frame in Frequency Domain, p. 12
$\mathbf{P}$	Mapping Relationship of Poincaré Maps, p. 55
$\mathbf{V}_{dq}$	Vector of Grid Voltages in dq-Reference Frame in Frequency Domain, p. 12

$\mathbf{a}$	Spatial Operator $e^{j\frac{2}{3}\pi}$, p. 11
$\mathbf{i}_{dq}$	Vector of Grid Currents in dq-Reference Frame, p. 12
$\mathbf{i}_{gabc}$	Three-Phase Grid Currents Vector, p. 11
$\mathbf{v}_{dq}$	Vector of Converter Pole Voltages in dq-Reference Frame, p. 12
$\mathbf{v}_{dq}$	Vector of Grid Voltages in dq-Reference Frame, p. 12
$\mathbf{v}_{gabc}$	Three-Phase Grid Voltages Vector, p. 11
$\mathbf{v}_{pabc}$	Three-Phase Converter Pole Voltages Vector, p. 11
μ	Zero Vector Apportion Ratio, p. 44
ω	Generic Angular Frequency, p. 11
ω_g	Grid Angular Frequency, p. 12
$\tilde{p}$	Oscillating Part of Instantaneous Active Power, p. 20
$\tilde{q}$	Oscillating Part of Instantaneous Imaginary Power, p. 20
d	Duty Cycle, p. 24
f_s	Switching Frequency, p. 23
i_D	Converter Diode Current, p. 31
i_L	Converter Inductor Current, p. 31
i_S	Converter Switch Current, p. 31
i_g	Grid Current, p. 4
i_g^*	Grid Current Reference, p. 3
i_{N0}	Common-Mode Current, p. 46
i_α, i_β	Currents in α-β Reference Frame, p. 19
k	Grid Voltage Gain for OCC with Voltage Measurement, p. 4
m_1	Rising Slope of Modulating Signal, p. 57
m_2	Falling Slope of Modulating Signal, p. 57
m_c	Rising and Falling Slopes of Carrier Signal, p. 57

p	Instantaneous Active Power, p. 20
q	Instantaneous Imaginary Power, p. 20
v_c	Carrier, p. 29
v_α, v_β	Voltages in α-β Reference Frame, p. 19
x^*	Fixed Point of Poincaré Maps, p. 56
x_a, x_b, x_c	Generic Variables in Static abc Reference for Park Transform Definition, p. 11
x_s	Space Vector of Generic Variable, p. 11

Chapter 1

Introduction

1.1 Background of the Problem

The challenging goals of keeping up to an ever increasing demand of electrical energy and on the reduction of greenhouse gas emissions are bringing about continuous efforts to improve the Electrical Systems in many perspectives. On the generation side, there is currently an expansion of the use of renewable energy sources [6], [7] and improvements on transmission infrastructure [8]. On the distribution side, most of the manufacturers of domestic and industrial electrical loads are making efforts to improve their efficiency, with the introduction of switched-mode power supplies since the 70's [9]. However, even with these efforts, most of the loads are still fed by uncontrolled rectifiers with diodes and capacitors which are a simple, cost effective and robust solution for AC/DC conversion but making these loads highly non-linear and drawing a highly pulsating current [10].

The highly pulsating currents when flowing through the impedances of the distribution circuits bring serious problems related to voltage drop and voltage distortion, affecting consumers connected to a common grid [11]. Other effects on grid are increased transformer, capacitor, motor or generator heating, additional acoustic noise from motors, malfunction of ripple control systems, protective relays, etc [12].

The European Standard IEC 61000-3-2 [13] has been set to define the limits for harmonics on electronic and electrical equipment with rated phase current up to 16 A, in which the equipments are categorized in four classes according to Table 1.1. A flow chart for classification of Electrical equipment conforming to this Standard and the Harmonics limits for each class are presented in Appendix A.1.

On the other hand, IEEE has a set of recommendations (IEEE 519-2014) [14] for distortion limits. The main difference compared to the IEC Standard is that the harmonics are measured at the Point of Common Coupling (PCC) of a given installation, so what is concerned are the harmonics of the installation reflected to

Table 1.1: European Standard IEC 61000-3-2: Classes of Equipments

Class	Equipments
A	Balanced 3-phase equipment; Household appliances excluding equipment identified as class D; Tools, excluding portable tools; Dimmers for incandescent lamps; Audio equipment; All other equipment, except that stated in one of the following classes.
B	Portable tools; Arc welding equipment which is not professional equipment.
C	Lighting equipment.
D	PC, PC monitors, radio, or TV receivers. Input power P $\leq$ 600 W.

the grid. The Current Distortion Limits for General Distribution Systems (120 V Through 69 000 V) and for General Subtransmission Systems (69 001 V Through 161 000 V) are summarized in Appendix A.2.

The solutions for harmonics issues can be classified into three classes [15], named First, Second and Third Classes. Examples of these solution classes are shown in Table 1.2.

Table 1.2: Solution for Harmonics Issues

Class	Solutions
First	Supplying the Loads from upstream; Grouping the Disturbing Loads; Supplying the Loads from separate transformers.
Second	Use of Transformers with special connections; Use of inductors for series connection in association with capacitor bank; Arrangement of System Earthing; Improvements on converter topology and/or control.
Third	Passive Power Filters; Active Power Filters; Hybrid Power Filters.

The first class is related to the distribution system, planning to determine how the installation can be modified to mitigate the effect of harmonics from disturbing loads on sensitive loads.

The second class of solutions is intended to mitigate or to confine harmonics produced by one ore more disturbing loads. The last solution of this class brings the solution to the inside of the load, which is related to philosophy of Standard IEC 61000-3-2.

The third class of solutions makes use of dedicated equipment to exempt the grid to provide a path to the harmonics generated by non-linear loads. A passive filter is a path of low impedance for specified harmonics, so that the harmonics generated by the load flows through the filter instead of flowing to the grid. Furthermore,

the passive filters can provide reactive power for PF correction. The Active Power Filters (APF) are converters which are controlled in such a way that voltage and/or current harmonics are produced with same amplitude but in opposite phase as those generated by the non-linear loads.

1.2 Cascade Control of Converters

Conventional analog and digital control techniques for converters are based on the cascade structure depicted in Figure 1.1-a, composed of an inner current controller R_{ig} and an outer DC bus voltage regulator R_{DC}. The output of R_{DC} defines the current reference amplitude I_g^* which is multiplied with the grid voltage measurement to generate the current reference i_g^*. The output of R_{ig} is compared to an unitary carrier to define the switch states of the converter for Pulse Width Modulation (PWM) based techniques or controlled by hysteresis band controller.

Even though these techniques are widely used to control power converters, they have disadvantages such as big input inductor size, switch stress, zero-crossing distortion, etc [16]. Furthermore they require grid and DC bus voltage sensors and current sensor. For digital-based techniques, the computational loads of their algorithms demand use of high-cost microprocessor-based devices, which is not suitable for low and medium power applications.

The One Cycle Control (OCC) technique, which is a non-linear PWM method and was proposed initially as an analog control method, realizes simultaneously PWM modulation and current control by the variation of carrier amplitude [17], [18] so that there is no explicit current loop (Figure 1.1-(b)). The output V_m of the DC bus voltage regulator R_{DC} defines the carrier amplitude , which is compared to the current measurement. This method requires only DC bus voltage and current sensors. The main advantages of this technique are simplicity, fast response, stability and robustness [18], [19].

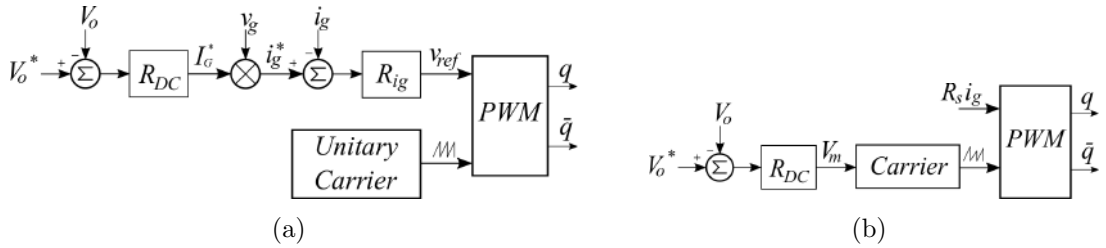


Figure 1.1: Schematics of Cascade Control Techniques for Converters: (a) Conventional Current Mode PI Control, (b) Current Mode One-Cycle Control.

1.3 Motivation

PFC Rectifiers and shunt APF are widely used solutions for PF correction and harmonics mitigation [20]. Even though these technologies have been applied since the 80's, these subjects are continuously studied concerning improvements on efficiency and costs, mainly focused in converter topologies and control improvements [21], [22]. On control side, the use of digital-based devices are increasingly spreading their application, since their cost is decreasing over time and at the same time their processing speed are on and on increasing [23].

Enhancements on OCC are also a current subject of study of control for PFC rectifiers and APF [24], [25]. In [26] the sawtooth carrier was replaced by a triangular carrier, allowing the simplification of control circuit and avoiding the need of any averaging scheme for the sensed current. However, no study has been done for stability analysis of this technique.

OCC has been digitally implemented in DSP for application in PFC [27] and APF [28]. In these techniques, instead of modulating the carrier amplitude, the output of R_{DC} divides the current measurement signal i_g generating the modulation signal m which is compared to an unitary carrier to generate the switch states - see Figure 1.2.

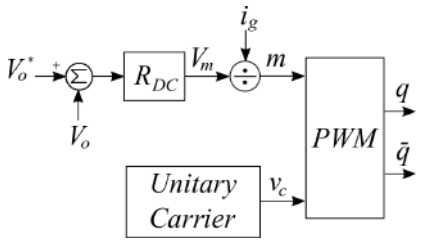


Figure 1.2: Schematics of Digital OCC Technique.

The algorithm of Digital OCC (DOCC) technique has easy implementation, so that systems with this control technique can employ low cost microprocessors to realize their control, what implies on system cost reduction.

Besides, the OCC technique can be modified to include grid voltage measurement with a gain k, as depicted in Figure 1.3 with resulting signal kv_g obtained by multiplication of sensed voltage v_g and gain k, for applications in Grid Connected Inverters (GCI) with $k < 0$ [29], [30], [31] and recently an analog OCC-based technique so-called Fast Response One-Cycle Control (FOCC) [32] has been proposed, which makes use of grid voltage measurements with $k > 0$ to improve the dynamic response and perturbation rejection of three-phase APF. However, the application of voltage measurements in OCC-based strategies is done in a stratified way. Aspects such as influence of k on system dynamics and on system stability are not described in a generalized approach.

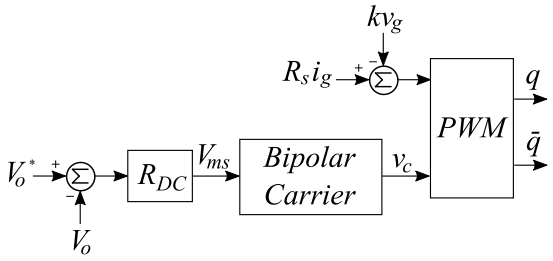


Figure 1.3: Schematic of Analog OCC with Grid Voltage Measurement.

Some improvements can be done on DOCC strategies, such as incorporation of Hybrid PWM, which has been done only for analog-based OCC strategies [5], and modification of strategy for compensation of inductive voltage drop [2].

1.4 Objectives

The main objective of this work is to analyze the application of DOCC strategies to PFC Rectifier and shunt APF to improve their actuation on correction of PF and mitigation of Total Harmonic Distortion (THD). The control will be implemented in a DSP to control a three-phase boost converter.

To achieve the main objective, the following specific objectives will be fulfilled:

- Modeling the power circuit of single-phase and three-phase PFC Rectifier and shunt APF;
- Application of Poincaré Maps approach to a OCC-controlled single-phase bidirectional boost converter model to analyze its stability;
- Derivation of averaged model of single-phase bidirectional boost converter to be used in frequency analysis of OCC and DOCC;
- Simulation on PSIM Environment of medium and lower power three-phase PFC Rectifier and shunt APF with DOCC strategies;
- Experimental implementation of lower power three-phase PFC Rectifier and shunt APF with DOCC strategies.

1.5 Contributions of the Dissertation

The main contributions of the Dissertation are listed below:

- Derivation of mandatory inductance value for stability of OCC strategies with triangular carrier;

- Proposal of a general approach for the application of grid voltage measurements to OCC techniques;
- Characterization of analog and digital OCC strategies through frequency analysis;
- Improvements on algorithm of feed-forward inductive voltage drop compensation concerning computational effort;
- Application of Hybrid PWM approach to DOCC.

1.6 Organization of the Dissertation

This text is composed of seven Chapters and two Appendices. Besides this Introductory Chapter, Chapter 2 presents a review on Active Compensation of Power Factor and Harmonics, approaching the classification of these solutions based on system and converter topology, and reviewing the main control found in Literature for these applications. Also, the project of standard PWM control methods are present, including a project of a Phase-Lock-Loop (PLL) circuit, mandatory part of these control strategies.

In chapter 3, it is done a review on OCC, starting from the early proposal of the analog technique, passing by the application of Resistor Emulator Approach with OCC to achieve unitary PF and low THD which can be applied to single and three-phase converters. Also, the three-phase OCC strategies are reviewed. Finally, it is presented the problem of inductive voltage drop, a inherent drawback of OCC strategies, and its remedy.

Chapter 4 shows comprehensively the contributions of this work, presenting also discussions about the improvements done in DOCC strategies.

In chapter 5, the results of simulations done in medium power level model of PFC Rectifier and shunt APF are provided, together with analysis of results.

Chapter 6 presents simulation and experimental results with comparative analysis of low scale model of PFC Rectifier and shunt APF, comparing these results also with those obtained in Chapter 5, to validate the control for application in low and medium power applications.

Chapter 7 concludes this work and presents suggestions for future work.

Appendix A shows the main aspects of the Standards for Harmonics Limits concerned in this work and Appendix B presents the deduction of the dynamic model of the H-bridge single-phase AC-DC converter controlled by OCC based on state-space averaging method.

1.7 Partial Conclusions

In this chapter it has been shown the general aspects of PF and Harmonics mitigation, covering the introduction to mainly used Standards worldwide, the main solutions. The OCC technique has also been introduced, together with motivations, objectives and contributions of the dissertation.

Chapter 2

Review on Active Compensation of Power Factor and Harmonics

2.1 Introduction

In this chapter it will be reviewed the general aspects of PFC Rectifiers and APF which are active solutions for PF and Harmonics correction. It will be studied their main aspects, covering general hardware and system topology classifications and also it will be shown a review on the control for these solutions. Furthermore, the design of conventional controls for each one of the solutions are presented.

2.2 PFC Rectifiers

Rectifiers are the most commonly used power electronics-based systems, with application ranging from adjustable-speed drive, Uninterruptible Power Supplies (UPS), High-Voltage Direct Current Transmission Systems, DC microgrids, general electronics loads, utility interfaces with renewable energy sources [33]. The main role of those converters is to make the interface between the AC grid and the DC bus. The DC bus voltage feeds electronic loads directly or eventually may be converted to AC by an DC-AC converter also known as inverter, or other DC voltage level by a isolated or non-isolated DC-DC converter as shown in Figure 2.1. The main concerns about the rectifiers are the harmonic content of input currents, low PF and slowly varying rippled DC output [34].

PFC Rectifiers are rectifiers with improved PF as well as harmonics content [35]. They work with a controlled converter operating at the Front-End to the load circuitry, so that they regulate the input grid current and output DC bus voltage. This alternative is highly applied in industrial application [11].

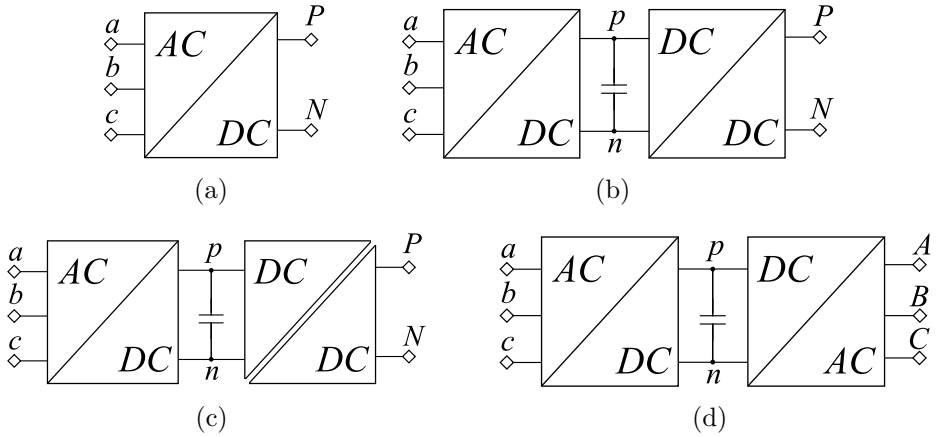


Figure 2.1: Schematics of Typical Converter Arrangement for Supplying Electrical Loads From Three-Phase AC Utility: (a) AC-DC Conversion, (b) AC-DC-DC Conversion with Non-Isolated DC-DC Converter, (c) AC-DC-DC Conversion with Isolated DC-DC Converter, (d) AC-DC-DC (Back-to-Back) Conversion.

2.2.1 Classification

The rectifiers can be classified by different aspects, for example energy flow direction, converter components [36] and converter topology. Based on energy flow direction, a rectifier can be either unidirectional, when the energy flows only from the AC side to DC side, or bidirectional, as the name suggests, allowing the energy flow in both directions. A rectifier can be classified as 1) Passive, when it is constructed by a diode bridge and passive elements for smoothing AC input current THD and DC voltage ripple [37]; 2) Hybrid rectifiers which are solutions based on passive rectifiers but combined with active solutions, for example an active element emulating a reactance behavior [38], bringing improvements in harmonic current level, output voltage ripple and converter volume; 3) Active PFC Systems, when the converter has forced commutation semiconductors, exclusively switching frequency passive components and regulated output voltage, such as the Direct Active Three-Phase PFC Rectifier proposed in [39].

Based on topology, the converter can be classified in Boost, Buck, Buck-Boost, Multilevel, Multipulse [36] as depicted in Figure 2.2.

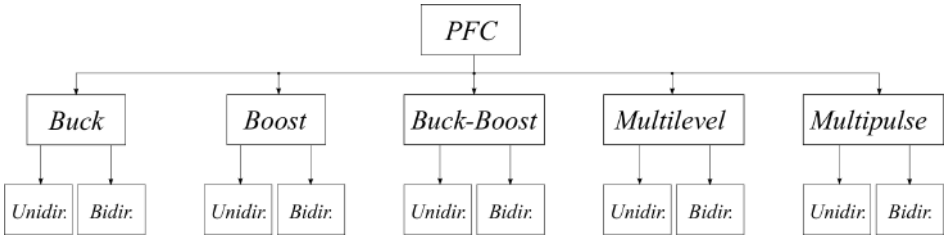


Figure 2.2: Classification of Rectifiers Based on Energy Flow Direction and Converter Topology.

2.2.2 Review on Control of PFC Rectifiers

The control of rectifiers can have three stages: DC bus control, current control and command pulses generation, or two stages when the current control and pulse generation are integrated.

The DC bus voltage control regulates the output voltage through regulation of active power flow. Traditional control techniques can be used such as PI [40] and PID control [41]. Furthermore sliding-mode control [42], fuzzy controllers [43], adaptive controllers [44], artificial neural network based controllers [45] can be used. These methods have good performance but with the expense of a high computational load. The output of DC bus controller defines the amplitude of input current.

For three stages strategies, the current can be controlled by several methods including PI [46], PID [47], PR [48], Neural Networks [49], Fuzzy Methods [49], Sliding Mode [50] and Adaptive [51]. The output of the current controller define the input signals for the PWM modulators to generate the command pulses for the switches. These methods have advantages of performance and robustness, but have some drawbacks as mandatory grid voltage measurement, control complexity and high computational cost of implementation.

Two stage methods have the current control and command pulse generation for the switches done together. The hysteresis control and OCC-based methods are examples of these control techniques. The fist is based on limiting the variation of the input current in control hysteresis bands, which can be fixed or variable. This method has the advantage of simple structure and good performance but has the disadvantages of use of grid voltage measurement for defining the current references, dead zones for input current close to zero and variable switching frequency [11]. The latter techniques are based on emulating a resistance by the converter, eliminating the need for grid voltage sensing. These techniques can be analog or digital based and have distinguishing characteristic of having no explicit current control loop and constant switching frequency.

Another advantageous characteristic of OCC-based techniques is the lack of Phase-Locked Loops (PLL) circuits, which reduces control complexity and allows the use of simple analog control circuitry or low cost microprocessor-based devices, therefore these techniques can be applied to PFC rectifiers for cost sensitive applications.

2.2.3 Control in dq-Frame for PFC Rectifiers

The conventional strategy for controlling a converter as a PFC rectifier makes use of two control loops: an external which controls the DC bus voltage an inner which controls the input currents and has a wider bandwidth compared to the outer loop.

The current control is realized with the three-phase currents transformed to the synchronous reference frame by Park Transform. A PLL circuit is used to provide the reference angle to direct and inverse Park Transforms.

In this subsection, the conventional control in dq-Frame of PFC Rectifiers is studied presenting its general aspects and design approach including current control design and PLL design.

The mesh (3.38) for converter of Figure 3.20 is rewritten in reduced matrix form neglecting the common mode voltage V_{N0} [52].

$$[\mathbf{v}_{gabc}] = L_g \frac{d}{dt}[\mathbf{i}_{gabc}] + [\mathbf{v}_{pabc}], \tag{2.1}$$

where $[\mathbf{v}_{gabc}] = [v_{ga} \quad v_{gb} \quad v_{gc}]^T$, $[\mathbf{i}_{gabc}] = [i_{ga} \quad i_{gb} \quad i_{gc}]^T$ and $[\mathbf{v}_{pabc}] = [v_{pa} \quad v_{pb} \quad v_{pc}]^T$ are the vector of grid voltage, grid current and pole voltages, respectively.

Given a three-phase set of variables $[x_a \quad x_b \quad x_c]$, its space vector can be mathematically defined as

$$\mathbf{x_s} = x_a + \mathbf{a}x_b + \mathbf{a}^2 x_c, \tag{2.2}$$

where x_a, x_b and x_c are the instantaneous values of the variables and $\mathbf{a} = e^{j\frac{2}{3}\pi}$ is a spatial operator.

Graphically, the space vector $\mathbf{x_s}$ can be seen in Figure 2.3 where for a symmetric system has amplitude X_s and rotates with frequency ω. This space vector can be represented in a static reference (abc) as so far, or be represented in a rotating reference frame where the phase and rotating frequency can be chosen in a convenient way.

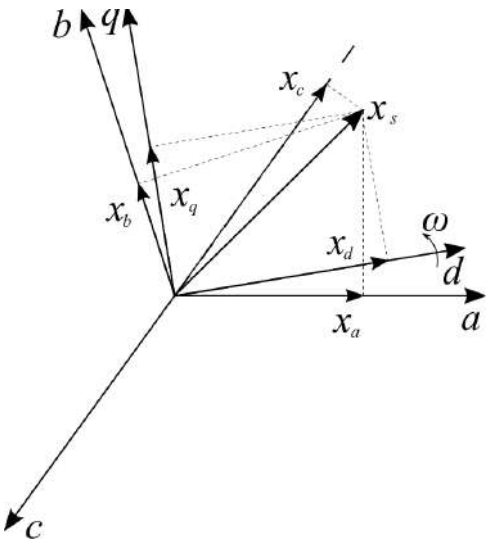


Figure 2.3: Space Vector of a Generic Three-Phase Set of Variables in Static abc and Rotating dq Reference Frames.

The transformation of a symmetric three-phase set from a static reference to a rotating one is done by the Park Transform, where its mathematical representation is

$$\begin{bmatrix} x_d \\ x_q \\ x_o \end{bmatrix} = \kappa \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2}{3}\pi) & \cos(\theta + \frac{2}{3}\pi) \\ \sin(\theta) & \sin(\theta - \frac{2}{3}\pi) & \sin(\theta + \frac{2}{3}\pi) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}, \tag{2.3}$$

in the form $[\mathbf{x}_{dq}] = T^{-1}[\mathbf{x}_{abc}]$ with $\kappa = \frac{2}{3}$ for equal amplitude transformation and $\kappa = \sqrt{\frac{2}{3}}$ for power invariant transformation.

Rewriting (2.1) considering (2.3) and choosing $\omega = \omega_g$ yields

$$T[\mathbf{e}_{gdq}] = L_g \frac{d}{dt} T[\mathbf{i}_{gdq}] + T[\mathbf{v}_{pdq}]. \tag{2.4}$$

Multiplying both sides by T_{-1} leads to

$$T_{-1}T[\mathbf{v}_{dq}] = T_{-1}(TL_g \frac{d}{dt}[\mathbf{i}_{dq}] + L_g \frac{d}{d\theta} T \frac{d}{dt}\theta[\mathbf{i}_{dq}]) + T_{-1}T[\mathbf{v}_{dq}]. \tag{2.5}$$

Resulting in

$$[\mathbf{v}_{dq}] = L_g \frac{d}{dt}[\mathbf{i}_{dq}] + \omega \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} [\mathbf{i}_{dq}] + [\mathbf{v}_{dq}]. \tag{2.6}$$

Applying Laplace Transform in (2.6) it becomes

$$[\mathbf{V}_{dq}(s)] = L_g s[\mathbf{I}_{dq}(s)] + \omega \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} [\mathbf{I}_{dq}(s)] + [\mathbf{V}_{dq}(s)], \tag{2.7}$$

with $\mathbf{V}_{dq}(s) = [V_d(s) \quad V_q(s)]^T$, $\mathbf{I}_{dq}(s) = [I_d(s) \quad I_q(s)]^T$ and $\mathbf{V}_{dq}(s) = [V_d(s) \quad V_q(s)]^T$ are the grid voltage, input current and pole voltages vectors in frequency domain respectively.

In Figure 2.4 is depicted the block diagram for dq currents obtained from (2.7). It can be seen that meshes d and are coupled, and the coupling terms are proportional to input inductance and grid frequency ω.

Neglecting harmonics and noise, in steady state the cross products becomes constants and are rejected by PI controllers. Furthermore the grid voltages can be considered as pertubation as well since its dynamics is much slower than current dynamics.

The complete control block diagram is shown in Figure 2.5.

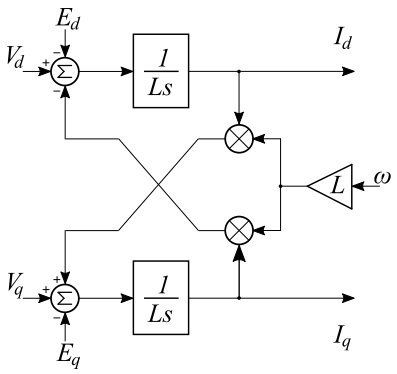


Figure 2.4: Block Diagram for dq Currents for Control in dq-Frame of PFC Rectifiers.

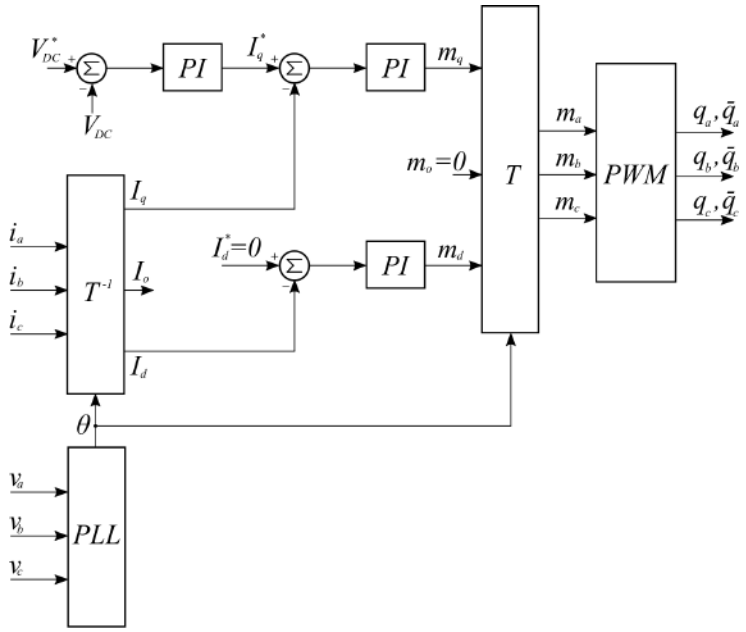


Figure 2.5: Block Diagram of Control in dq-Frame for Three-Phase Full-Bridge PFC Rectifier.

2.2.3.1 Current Control Design

The current control loop for currents d and q can be represented as in Figure 2.6. The PI controllers for axes d and q define the input signals m_d, m_q for the modulator and the PWM block is modeled as a gain V_{DC}.

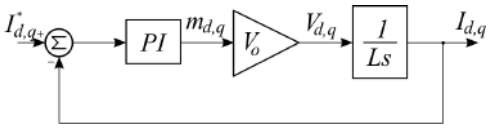


Figure 2.6: Block Diagram of Current Loop Control for Control in dq-Frame of PFC Rectifiers.

The open-loop transfer function is given by

$$H_{ol}(s) = \left(K_p + \frac{K_i}{s}\right) V_{DC} \frac{1}{sL}. \tag{2.8}$$

The closed loop transfer function can be written as

$$H_{cl}(s) = \frac{\frac{K_p V_{DC}}{L} s + \frac{K_i V_{DC}}{L}}{s^2 + \frac{K_p V_{DC}}{L} s + \frac{K_i V_{DC}}{L}}. \tag{2.9}$$

From (2.9) It can be seen that the current loop has a zero on the left half side of complex plane. The presence of this zero increases the system overshoot and the rise time but has little influence on settling time [53].

First the (2.9) is broken up

$$H_{cl}(s) = \frac{\frac{K_i V_{DC}}{L}}{s^2 + \frac{K_p V_{DC}}{L} s + \frac{K_i V_{DC}}{L}} + \frac{\frac{K_p V_{DC}}{L} s}{s^2 + \frac{K_p V_{DC}}{L} s + \frac{K_i V_{DC}}{L}}. \tag{2.10}$$

In [54] it has been shown that a second order system with a zero can have the effect of zero mitigated by choosing $\zeta > 1$, i.e., making the system over-damped. Then controller design is done by ignoring the zero on (2.10) becoming

$$H_{cl}(s) = \frac{\frac{K_i V_{DC}}{L}}{s^2 + \frac{K_p V_{DC}}{L} s + \frac{K_i V_{DC}}{L}}. \tag{2.11}$$

Comparing it with a generic second order equation

$$H_g(s) = \frac{s\frac{\omega_n}{\alpha\zeta} + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{2.12}$$

The expressions for the PI controllers are given as

$$K_p = \frac{2\zeta\omega_n L}{V_{DC}}, \tag{2.13}$$

$$K_i = \frac{\omega_n^2 L}{V_{DC}}. \tag{2.14}$$

An over-damped system has its dynamics approximated by a first order system with time response given by

$$c(t) = 1 - e^{-(\zeta - \sqrt{\zeta^2 - 1})\omega_n t}. \tag{2.15}$$

The effect of the zero increases the dynamic response of the system, as seen before. Since the control goal is to make the system time response equal to that of the OCC control, it can be found that the system time response can be approximated by

$$\tau_{PI} \approx \frac{1}{16\omega_n(\zeta - \sqrt{\zeta^2 - 1})}. \tag{2.16}$$

2.2.3.2 PLL design

The Block Diagram of d-PLL in Figure 2.7.

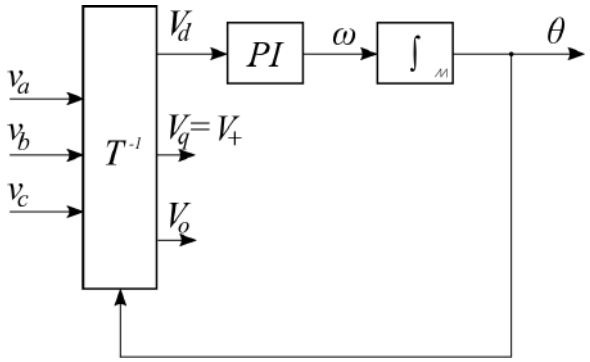


Figure 2.7: Block Diagram of d-PLL.

The small signal model for small changes $\Delta\theta$ for the PLL of Figure 2.7 is depicted in Figure 2.8.

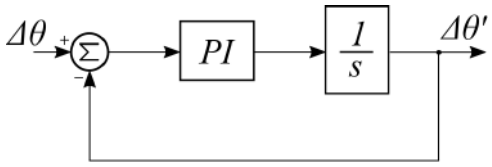


Figure 2.8: Block Diagram of d-PLL - Small Signal Model.

The open loop transfer function is given by

$$H_{olPLL}(s) = \left(K_{pPLL} + \frac{K_{iPLL}}{s}\right)\frac{1}{s}. \tag{2.17}$$

The closed loop transfer function can then be got

$$H_{cl}(s) = \frac{K_{pPLL}s + K_{iPLL}}{s^2 + K_{pPLL}ss + K_{iPLL}}. \tag{2.18}$$

As in the current controller design, the closed loop loop of the PLL for small signal analysis is a second order transfer function with a zero in the left half plane. The project is proceed with a damping ratio $\zeta > 1.0$ as well aiming to mitigate the effect of the zero on the system dynamical response. With this condiction, the controller is projected as if the zero does not exist.

Comparing the closed loop transfer function in (2.18) with (2.12) results in

$$K_{pPLL} = 2\zeta\omega_n, \tag{2.19}$$

$$K_{iPLL} = \omega_n^2. \tag{2.20}$$

The settling time can be approximately calculated by

$$t_s = \frac{4.0}{\zeta \omega_n}. \tag{2.21}$$

Choosing t_s equals to one-quarter of the period $T_g = 16.67ms$ leads to

$$\zeta \omega_n = 960.0. \tag{2.22}$$

Choosing $\zeta = 2.0$, therefore

$$\omega_n = 480.0. \tag{2.23}$$

Then the values of K_{pPLL} and K_{iPLL} are easily determined from (2.19)-(2.20).

2.3 APF

APF can provide harmonic and reactive content for non-linear loads, exempting the grid to provide a path to the harmonics generated by these loads. APF have merits of dynamic and adjustable compensation, smaller size and robustness for resonance.

2.3.1 Classification

APF can be classified based on converter type: Voltage Source Inverter (VSI) or Current Source Inverter (CSI); system topology: shunt, series or combination of both; and on converter topology: three wire and four wire [55].

CSI-based APF's are characterized by a constant DC-side current and an inductor as an energy storage element as illustrated in Figure 2.9-a. These converters are considered very good at synthesizing a current reference, sufficiently reliable, but have higher losses and require higher values of parallel ac power capacitors.

VSI-based APF's, on the other hand, have constant DC voltage and a capacitor as energy storage element as shown in Figure 2.9-b. These solutions have several advantages such as excellent current control capability, easy protection and high reliability over CSI-based APF's [56].

The series APF is connected upstream to the load, in series with the utility network conventionally using matching transformers [57] as shown in Figure 2.10-a. Transformerless series APF approaches are presented in [58]. These devices are used to eliminate voltage harmonics, to balance and regulate the terminal voltage of the load or line, to reduce negative-sequence voltage.

The shunt filters are connected in parallel to the grid at the PCC as shown in Figure 2.10-b. They are used to eliminate current harmonics and operate injecting equal compensating currents, opposite in phase, to cancel harmonics and/or reactive

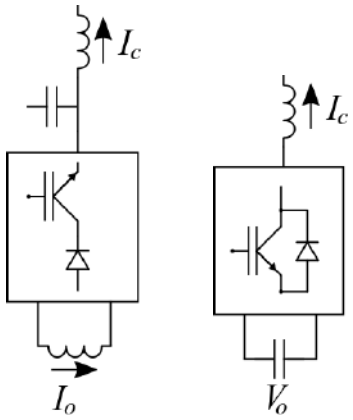


Figure 2.9: APF Classification based on Converter Type: (a) CSI-based APF (b) VSI-based APF

components. They can also provide reactive power compensation (STATCOM) and balance unbalanced currents.

The combination of series and shunt APF gives rise to the Unified Power Quality Conditioner, made of the combination of both topologies. The storage element is shared between the two converters, one operating as series filter and the other operating as shunt filter as depicted in Figure 2.10-c. They compensate voltage and current harmonics, being considered as an ideal filter. The drawback is their larger cost and control complexity.

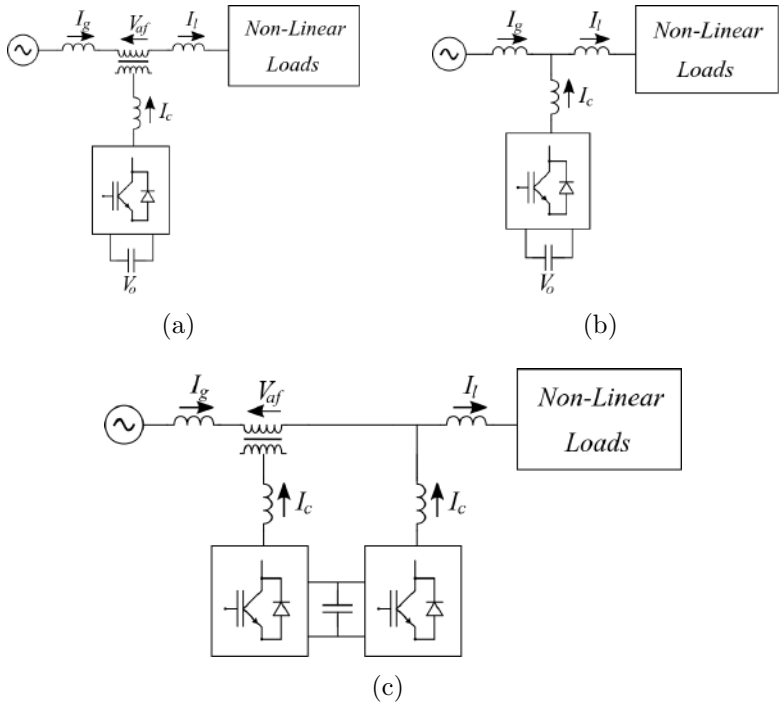


Figure 2.10: APF System Topologies: (a) Shunt APF, (b) Series APF (b) Shunt-Series APF - Unified Power Quality Conditioner - UPQC.

The three-phase Shunt APF may be classified based on converter topology as three-wire - used to compensate non-linear loads harmonics in three-phase three-wire systems, and four-wire - used to compensate harmonics and fundamental and harmonic zero sequence currents caused by load imbalance and triplen harmonics caused by single phase loads in neutral line. For each type, the APF's can be further classified as two-level or multilevel.

2.3.2 Review on Control of Shunt APF

The control techniques for VSI-based Shunt APF can be classified following the approach presented in [59]:

1. Harmonic extractor-based strategies (HEBS): the non-linear load current is measured and its content is defined explicitly, so that the current reference for the APF is characterized. Several techniques can be classified as HEBS including pq Theory [60], dq Method [61], Synchronous Detection Method [62], Flux-Based [63], Notch Filter Method [64], Adaptive Filter [65], Artificial Neural Network [66], Fast Fourier Transform (FFT)[67], Recursive Fourier Transform[68] and Wavelet [69]. These control techniques performance depends on the speed and accuracy of the calculation of harmonic components of the non-linear loads and may demand high-speed microprocessors. Furthermore, the effectiveness of these techniques relies on the current controller performance;

2. Balanced energy based schemes (BEBS), or indirect method: the supply currents are directly measured and the APF is controlled so that the grid currents are to be sinusoidal [70] [71], [72], [73], [74]. Their performances depend on how fast the system reaches the equilibrium state [72]. Since these techniques do not employ Harmonic extractors, they can prevent inaccurate tracking of the harmonic detector.

The DC bus voltage is regulated so that the voltage keeps at a suitable level, hence the grid must supply some active power to compensate the APF losses. Several control techniques are reported to do this task: PI controllers, feed-forward schemes for compensating the power grid voltage fluctuation[75], adaptive control[76], hybrid control combining PI and sliding mode[72]. These controllers output sets the active power to be draw by the converter for HEBS or the reference active grid current for the current regulator for BEBS.

Several explicit current control techniques (APF current for HEBS and grid current for BEBS) are found in literature. For HEBS techniques: PI control [77], dead-beat control [78], hysteresis control [79], sliding mode control [80], adaptive

control [81], resonant control [82], repetitive-based control [83]. In BEBS techniques: resonant controller per phase[72], PI-VPI [73]. The PI controller is stated to be ineffective to APF current control, due to control bandwidth limitations [73]. The dead-beat control method performance relies on knowledge of the APF parameters. The other techniques have the drawback of demanding high-speed processors do compute their algorithms.

On the other hand the OCC-based strategies [74], which are implicit current control techniques, use the output of the DC bus voltage controller as the carrier amplitude reference for the PWM modulation, which has implicitly the reference active grid current in it. The grid current is sensed and compared to the modulated carrier with the control goal to keep the average of the grid current within one cycle proportional to grid voltage. The conventional OCC-based strategies do not employ grid voltage measurements, which simplifies the system and reduces its cost.

Since there is neither harmonic extractor nor explicit current controllers in the structure of the OCC applied to APF, these techniques can be implemented in low cost microcontrollers, therefore these techniques are very suitable to APF for cost sensitive applications.

2.3.3 pq-PWM Control for APF

For controlling APF the conventional strategy is based on pq theory, which is a HEBS technique, as seen in Subsection 2.3.2. The technique was first proposed by [84], and is widely used in practical applications [85]. It is based on calculation and extraction of instantaneous harmonics and reactive content of the load, and selection of the content to be supplied by the converter.

From a set of voltages and currents in stationary reference frame the instantaneous power can be calculated as follows

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}, \tag{2.24}$$

where power p corresponds to the instantaneous power that realizes Work, while q is the imaginary power which does not contribute to power flow but circulates between phases.

Furthermore, each power can be separated into two parts:

$$p = \bar{p} + \tilde{p}, \tag{2.25}$$

$$q = \bar{q} + \tilde{q}. \tag{2.26}$$

The $\bar{p}$ and $\tilde{p}$ quantities represent the average and oscillating parts of p, whereas $\bar{p}$ and $\tilde{p}$ are the average and oscillating parts of q.

By manipulating (2.24), the currents in $\alpha\beta$ stationary reference frame can be derived from

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} p^* \\ q^* \end{bmatrix}. \tag{2.27}$$

This is the general mathematical base for the pq theory applied to APF. The control structure for a three-phase APF is shown in Figure 2.11. First the load voltages and currents are measured and transformed into $\alpha\beta$ stationary reference frame. Then the instantaneous powers p and q drawn by the load are calculated from (2.24), and from these values the reference powers to be drawn by the converter are defined. In this study for a proper comparative study between OCC and pq-PWM APF's these values are selected as expressed by (2.28), where p_{loss} is the converter power losses

$$\begin{aligned} p^* &= \tilde{p} + p_{loss}, \\ q^* &= \bar{q} + \tilde{q}. \end{aligned} \tag{2.28}$$

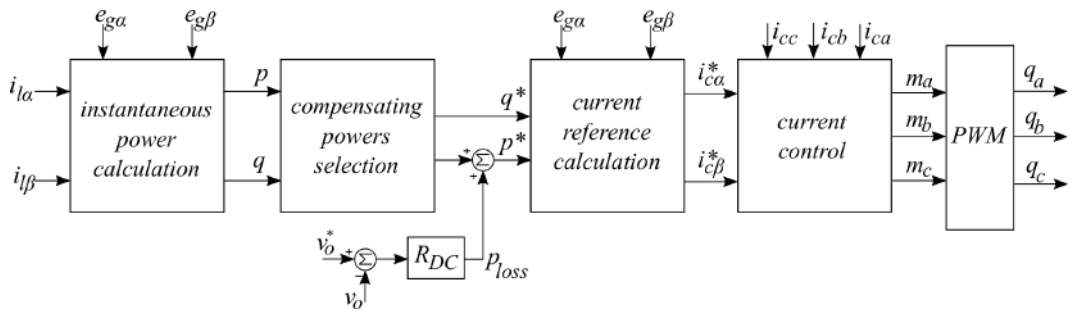


Figure 2.11: Block Diagram of pq-PWM APF.

From (2.27) the reference converter currents $i_{c\alpha}^*$ and $i_{c\beta}^*$ are defined to the current controllers. Two different current control strategies are are selected: PI control in dq reference frame and hysteresis-band current control.

2.3.3.1 PI Control

On this approach, the reference currents $i_{c\alpha}^*$ and $i_{c\beta}^*$ are transformed into dq0 rotating reference frame from (2.3), resulting in current references i_{cd}^* and i_{cq}^*. Then they are controlled by PI regulators.

Since PI controllers have a narrow bandwidth and the current references i_{cd}^* and i_{cq}^* are composed of high-order harmonics, the effectiveness of these controllers in

this application limited as discussed in [73]. Another drawback of this technique is the need for the use of PLL circuits, used in the transformation from stationary reference frame into rotating reference frame.

2.3.3.2 Hysteresis-Band

The Hysteresis controller, or Bang–Bang Controller, is a very popular control technique due to its simplicity of implementation, fast transient response, suitable stability and high accuracy [86]. It is based on the switch of an plant input between two states on or off to control an output that provides hysteresis as shown in Figure 2.12

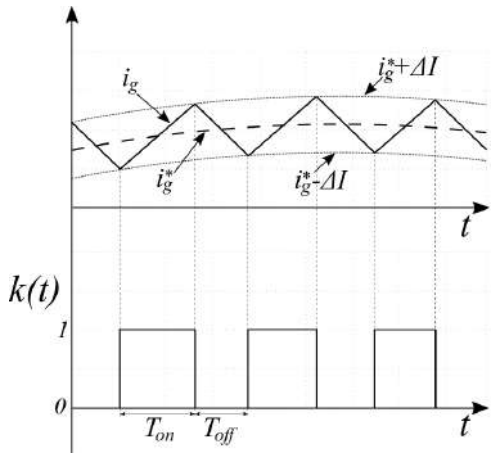


Figure 2.12: Hysteresis Control Principle.

In our case, the plant outputs are the measured converter currents and inputs are the switch states q_a, q_b, q_c. Each current is controlled individually: when a converter phase current reaches the upper limit the switch state q_x goes to zero, similarly when the current reaches the lower limit the switch state q_x goes to one.

Another advantage of the application of this control technique for current regulation is the no need for a PLL structure.

The main disadvantages of the Hysteresis-Band Current Control is the variable switching frequency - causing audible noise, sub-harmonics and difficulties to design the input filter, and increased switching losses [87].

2.4 Partial Conclusions

In this chapter the general aspects of PFC Rectifiers and APF have been reviewed, with general hardware and system topology classifications and also on the control techniques for each solution. The design of conventional control methods for each one of the solutions were presented.

Chapter 3

Review on One Cycle Control

3.1 Introduction

As seen in last Chapter, several control techniques can be applied to cascaded control of converters. The OCC technique, as seen, has several advantages over other control methods: simpler control structure, robust and stable operation with spontaneous dynamic response, and can be implemented by analog and digital approaches for Single-Phase and Three-Phase PFC Rectifiers, APF and GCI.

In this chapter, a general review on OCC is done, covering the theory of the technique as it was proposed by [17], the implementation of Resistor Emulator approach with OCC to Single-Phase converters with applications, the OCC approaches for Three-Phase converters with applications, finishing up with the phase angle displacement associated with the inherent inductive voltage drop and the existing solutions for this drawback of the technique.

3.2 Analog OCC

In this section, the analog implementation of OCC technique is didactically introduced from its principle, as proposed in [17], showing its main differences to conventional PWM technique. Further, this technique is used to achieve the Resistor Emulator approach, which states the control goal to keep the input voltage and current proportional.

In Figure 3.1 it is shown the schematic of a generic switch, operating at constant frequency f_s, with input $x(t)$ and output $y(t)$. It is assumed that the switching frequency f_s is much higher than the frequencies of $x(t)$ and $y(t)$. Therefore within one cycle, the input and output signal may be considered as constants.

The switch has its state defined by the switching function $k(t)$ expressed by (3.1).

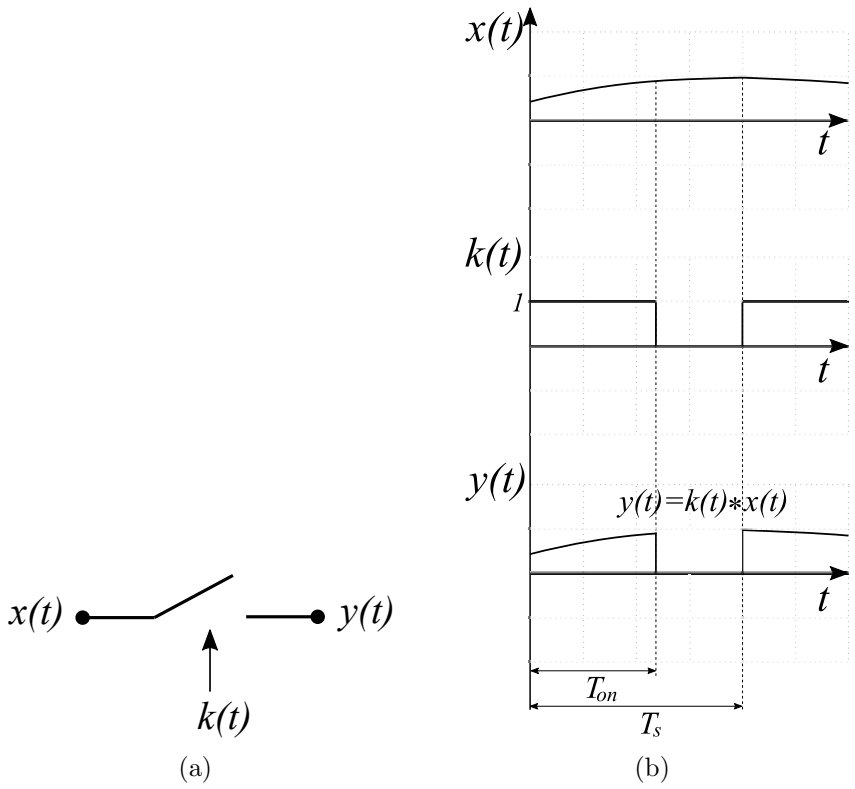


Figure 3.1: Generic Switch: (a) Schematics, (b) Switching Pattern.

$$k(t) = \begin{cases} 1 & 0 < t < T_{on} \\ 0 & T_{on} < t < T_s \end{cases}, \tag{3.1}$$

where:

- T_s is the switching period
- T_{on} is time that the switch remains in its closed state

The period that the switch remains open is called $T_{off} = T_s - T_{on}$ and the duty cycle $d = \frac{T_{on}}{T_s}$ is defined as the ratio between the time the switch is on and the switching period, thus respecting the limits

$$0 \leq d \leq 1. \tag{3.2}$$

The output $y(t)$ can be defined in the form [1]

$$y(t) = \begin{cases} x(t) & 0 < t < T_{on} \\ 0 & T_{on} < t < T_s. \end{cases} \tag{3.3}$$

[1] This is valid for a single switch.

In this case, the average value $\bar{Y}$ of the pulsed output $y(t)$ can be controlled by the variation of the duty cycle d as shown in Figure 3.2. This technique is called Pulse-Width Modulation (PWM).

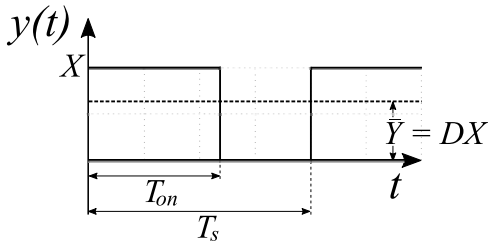


Figure 3.2: Pulse-Width Modulation Technique Principle.

The switching pattern can be determined by comparing the signal $v_{ref}(t)$ with a periodic carrier signal $v_c(t)$ of frequency f_s - this process can be seen in Figure 3.3. It is assumed that the frequency of v_c is much higher than the frequency of signals $x(t)$ and v_{ref}, therefore $x(t)$ and $v_{ref}(t)$ may be considered constants:

$$\begin{cases} x(t) = \bar{X} \\ v_{ref}(t) = \bar{V}_{ref} \end{cases} . \tag{3.4}$$

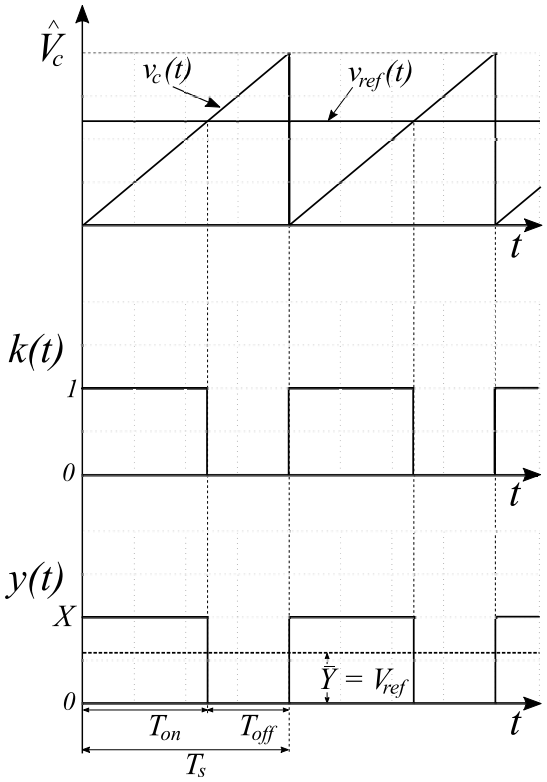


Figure 3.3: Generation of Output Pulse with PWM Technique.

In the time interval in which the carrier v_c is bigger than reference signal v_{ref} the switch keeps off, i.e., $k(t) = 0$. When v_{ref} gets higher than v_c the switch turns on, i.e., $k(t) = 1$.

The duty cycle d therefore can be put as a function of the amplitudes of v_{ref} and v_c

$$d(t) = \frac{v_{ref}(t)}{\hat{V}_c}. \tag{3.5}$$

For the case when the carrier amplitude is unitary the (3.5) becomes

$$d(t) = v_{ref}(t). \tag{3.6}$$

The average of output signal $y(t)$ within one cycle is calculated as

$$\bar{Y} = \frac{1}{T_s}\int_0^{T_s} y(t)\,\mathrm{d}t = \frac{1}{T_s}\int_0^{T_s} k(t)x(t)\,\mathrm{d}t = \frac{1}{T_s}\int_0^{T_{on}} x(t)\,\mathrm{d}t. \tag{3.7}$$

Considering (3.4) it leads to

$$\bar{Y} \approx \bar{X}\frac{1}{T_s}\int_0^{T_{on}} \mathrm{d}t = \bar{X}d(t). \tag{3.8}$$

Replacing (3.6) in (3.8) and considering (3.4) leads to

$$\bar{Y} = \bar{X}\bar{V}_{ref}. \tag{3.9}$$

Hence, the average value of the output $y(t)$ is the product of the average values the of input $x(t)$ with the reference signal $v_{ref}(t)$, hence this relation is nonlinear. If there is a disturbance in $x(t)$, the output $y(t)$ is affected but this will be corrected only after the actuation of the control structure for the update of $v_{ref}(t)$.

In OCC modulation, on the other hand, the output $y(t)$ is integrated such that its value is exactly equal to the integration of the reference value $v_{ref}(t)$, i.e.

$$\int_0^{T_s} y(t)\,\mathrm{d}t = \int_0^{T_s} k(t)x(t)\,\mathrm{d}t = \int_0^{T_{on}} x(t)\,\mathrm{d}t = \int_0^{T_s} v_{ref}(t)\,\mathrm{d}t. \tag{3.10}$$

Then the average value of the output $y(t)$ is equal to average of the reference value $v_{ref}(t)$ in each cycle, i.e.

$$\bar{Y} = \frac{1}{T_s}\int_0^{T_s} y(t)\,\mathrm{d}t = \frac{1}{T_s}\int_0^{T_s} v_{ref}(t)\,\mathrm{d}t = \bar{V}_{ref}. \tag{3.11}$$

Therefore, this technique ensures the average value of the switch output is equal to the average of the reference value in each cycle so that the output is controlled instantaneously within one cycle. Hence the terminology *One Cycle Control*. This technique ensures switch input-output conversion linearity, input disturbance rejection and excellent dynamic response [32]-[88].

The OCC modulation process is shown in Figure 3.4.

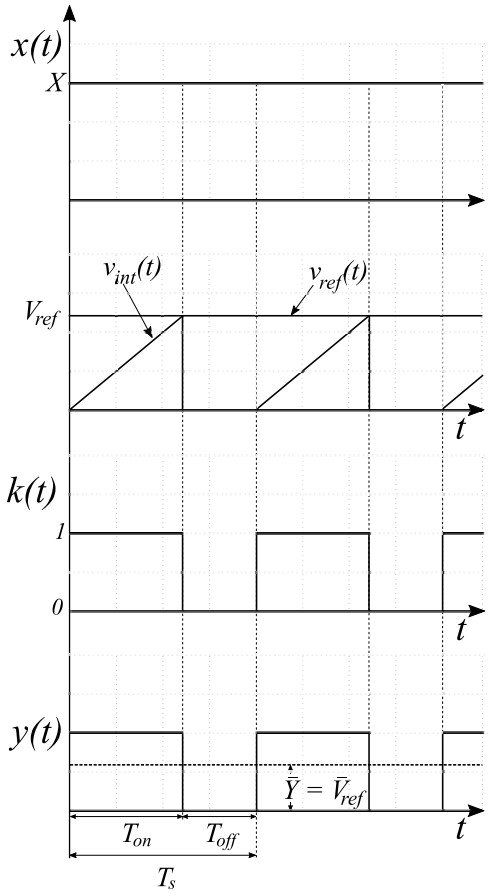


Figure 3.4: OCC Modulation Operation: Switch Input, Carrier, Switch Gate Signal and Switch Output.

The quantity $v_{int}(t)$ is the carrier of the general OCC technique and is generated by the integration of the output value $y(t)$, i.e.

$$v_{int}(t) = \int_0^{T_s} y(t)\,\mathrm{d}t = \int_0^{T_{on}} x(t)\,\mathrm{d}t. \tag{3.12}$$

The analysis of Figure 3.4 and (3.12) indicates that the slope of the carrier depends on the input value $x(t)$. But, on the other hand, the output $y(t)$ is integrated till it reaches $v_{ref}(t)$. Therefore the duty-cycle d is modulated such that the relationship $\bar{Y} = \bar{V}_{ref}$ is always satisfied within one cycle, even with perturbations in $x(t)$ or $v_{ref}(t)$ inside a cycle.

This technique was first proposed with an analog implementation, with the circuit of Figure 3.5. The circuit consists of an integrator, a comparator, a constant-frequency clock, and a flip-flop circuit for switch drive.

In the next section, the approach of the resistor emulation, which can be achieved with OCC, is studied as well as a general procedure for the design of average current mode control laws for single-phase topologies operating in CCM.

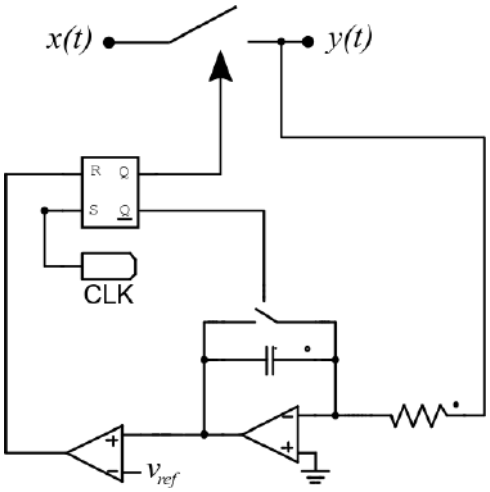


Figure 3.5: Implementation Circuitry for OCC.

3.2.1 Resistor Emulation

When a converter is controlled in such a way that its output voltage is regulated at a desired value and its input current has the same waveform as its input voltage, this converter is said to be controlled by the Resistor Emulator approach [89], since its control goal is to make the converter emulate a resistor as illustrated in Figure 3.6. This approach is extensively applied to PFC Rectifiers with several control techniques including Voltage-Follower Control [90], Multiplier Approach Control [91] and OCC-based techniques [92], [18]. It can also be applied for APF control [93].

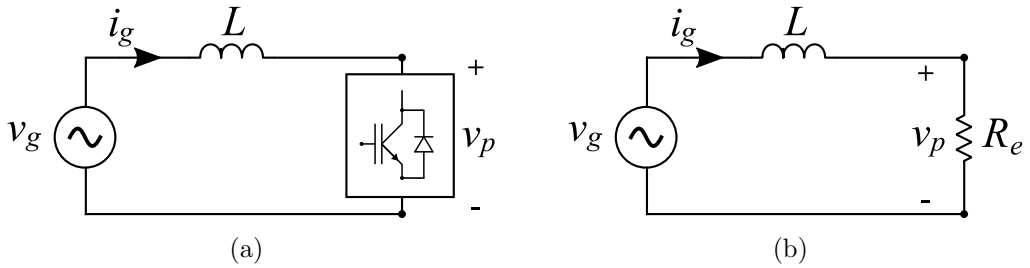


Figure 3.6: The Principle the Resistor Emulator Approach for Control of a Single-Phase Converter.

The control goal is to keep the average of its input current $i_g(t)$ proportional to the input voltage $v_g(t)$, i.e.

$$\frac{v_g(t)}{\bar{I}_s} = R_e > 0, \tag{3.13}$$

where R_e is an emulated resistance "seen" by the source.

For DC-AC conversion, the control goal is to keep input voltage and current in opposite phase, i.e., making the converter to emulate a negative resistor

$$\frac{v_g(t)}{\bar{I}_s} = R_e < 0. \tag{3.14}$$

The OCC-based techniques rests on cycle-by-cycle integration of control variables and their control laws are derived from the quasi-steady-state approach, which is built based on the assumption that input voltage being constant within a switching cycle - this is derived on the supposition that the switching frequency f_s much higher than the grid frequency f_g. This approach was proposed in [94] for an analog control technique for converters operating in CCM called Non-Linear Carrier Control (NLC).

Considering the single-phase case, a generalized input-output relationship for a converter operating in CCM is given by

$$v_g = f(d)V_o, \tag{3.15}$$

where v_g is the grid voltage within one switching period, V_o is the output voltage and $f(.)$ is the converter quasi-steady-state transfer function.

Admitting the converter emulates a resistor and therefore substituting (3.13) in (3.15) with the grid current sensor output resistance R_s considered, it is obtained

$$R_s\bar{I}_g = f(d)V_m = v_c, \tag{3.16}$$

where $V_m = R_sV_o/R_e$ is the output of the DC-bus voltage regulator. The term $v_c = f(d)V_m$ is realized by a carrier with amplitude equal to V_m and its waveform depends on the form of $f(.)$.

In [95] it was presented a family of constant-switching frequency PWM controllers for single-phase PF correction circuits operating in CCM with current mode control based on resistor emulator and quasi-steady-state approach, introducing a methodology for developing these control techniques for various converters topologies and applying them with the Generalized PWM [1]. The circuit for implementation of the generalized PWM is shown in Figure 3.7.

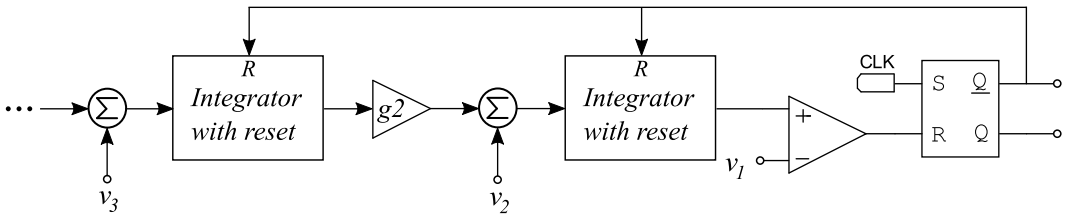


Figure 3.7: Generalized PWM Circuit - Adapted from [1].

The modulation of the generalized PWM is realized based on

$$v_1 = v_2d + g_2v_3d^2 + ... \tag{3.17}$$

for defining the flip-flop output Q pulse width or

$$v_1 = v_2(1-d) + g_2 v_3 (1-d)^2 + ..., \tag{3.18}$$

for defining the flip-flop output $\bar{Q}$ pulse width.

Therefore (3.16) can be manipulated to the form of (3.17) to realize the modulation of d.

In [96] it is presented a general procedure with four steps for the design of average current mode control laws for single-phase topologies operating in CCM:

1. The objective of the control of PFC is to emulate a equivalent resistance:

$$\bar{I_g} = \frac{\bar{V_g}}{R_e}. \tag{3.19}$$

2. The CCM steady-state input-output voltage relationship for the given topology is determined and substituted for v_g, in the above equation;

3. Using the PWM-switch model, the relationships between the branch currents (inductor, diode, switch) and input current are derived for the given topology;

4. Substituting the results of Steps 3 and 2 in Step 1, a set of solution candidates are obtained.

To obtain the average of the currents for solution candidates, several averaging schemes are normally employed in conventional OCC strategies [94], [96], [97], [27].

3.3 Single-Phase OCC

In this section the resistor emulator approach for control of converters is applied to OCC technique to control Unidirectional and Bidirectional Rectifiers and Grid Connected Inverters.

3.3.1 Unidirectional Rectifier

Considering the Unidirectional AC-DC Boost converter in Figure 3.8, with a DC-DC converter placed between the diode bridge and the output capacitor.

Applying the methodology described in [96] for this converter, it is obtained firstly the resistance emulation law

$$|\bar{I_g}| = \frac{|v_g(t)|}{R_e}. \tag{3.20}$$

The input-output voltage relationship is given by

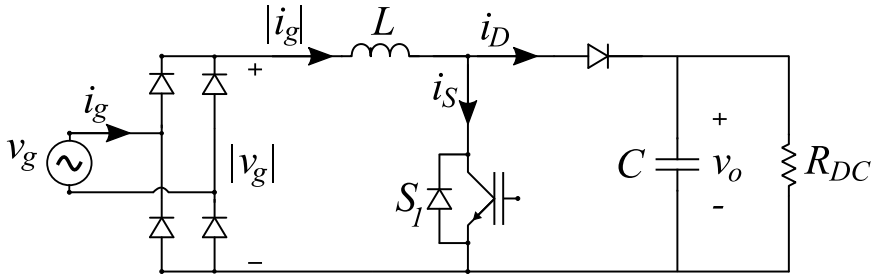


Figure 3.8: Model of Single Phase Unidirectional Boost Rectifier.

$$\frac{V_o}{|\bar{V}_g|} = \frac{1}{1-d}. \tag{3.21}$$

The relationship between input and inductor currents is given by

$$\bar{I_L} = |\bar{I}_g|. \tag{3.22}$$

The relationship between diode and inductor currents is

$$\bar{I_D} = |\bar{I}_g|(1-d). \tag{3.23}$$

Similarly for switch current

$$\bar{I_S} = |\bar{I}_g|d. \tag{3.24}$$

Substituting (3.20) in (3.21) and taking account of (3.22)-(3.24), a set of solution candidates are obtained and can be summarized in Table 3.3.1.

Table 3.1: Solution candidates for resistance emulation control goal for Unidirectional DC-DC Boost.

Current	Solution
inductor	$\bar{I_L} = \frac{V_o}{R_e}(1-d)$
switch	$\bar{I_S} = \frac{V_o}{R_e}(1-d)d$
diode	$\bar{I_D} = \frac{V_o}{R_e}(1-d)^2$

The carrier waveforms $v_c(t)$ for each solution from 3.3.1 are obtained simply by replacing d by t/T_s in each solution candidate. The inductor current one has the simplest carrier waveform, a negative slope linear carrier with peak value of V_m, described by $V_m(1-t/T_s)$ as shown in Figure 3.9-(a). The solution candidate of average switch current has a parabolic waveform carrier with its peak value of $V_m/4$ in the center of the switching cycle described by $V_m t/T_s(1-t/T_s)$ as illustrated in Figure 3.9-(b). The carrier waveform for the control by average diode current is a negative slope quadratic waveform with peak value of V_m described by $V_m(1-t/T_s)^2$ as depicted in 3.9-(c).

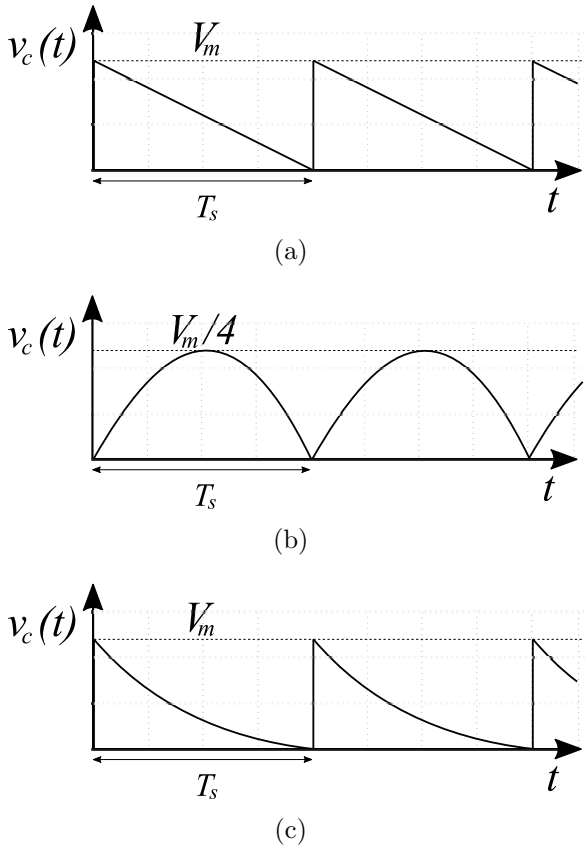


Figure 3.9: Carriers of Control with Unipolar OCC: (a) Average Inductor Current, (b) Average Switch Current and (c) Average Diode Current.

The schematic of unipolar OCC with resistor emulator by average inductor current is shown in Figure 3.10(a), where the DC-bus regulator defines the amplitude of the carrier, which can be generated by a circuit consisting of a integrator with reset

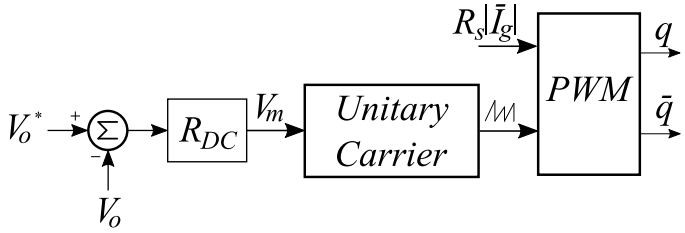


Figure 3.10: Schematic of Unipolar OCC with Resistor Emulator with Average Inductor Current.

Making d explicit from (3.21)

$$d = \frac{|v_g(t)|}{V_o}. \tag{3.25}$$

Therefore, the current control is realized such that the duty-cycle d is modulated to follow $|v_g(t)|$, and to keep the DC-link voltage at its reference value, since the DC bus is fed by the input current.

In Figure 3.11 it is shown the result for the converter of Figure 3.8 controlled by OCC with the resistor emulator approach. The input current is approximately sinusoidal and in phase with the input voltage, therefore the resistor emulator approach is achieved.

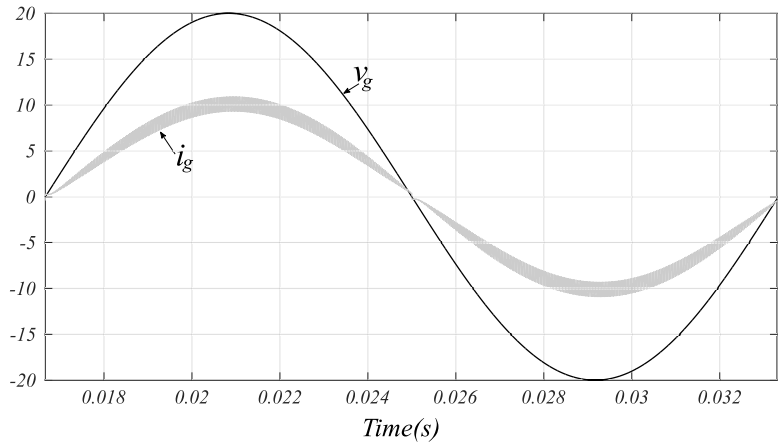


Figure 3.11: Single-Phase Unidirectional Boost Rectifier with OCC: Input Voltage (5 V/div.) and Input Current (1 A/div.).

3.3.2 Bidirectional Rectifier

The model of a Single-Phase bidirectional Rectifier is shown in Figure 3.12 and it consists of a Single-Phase AC source v_g and a Full-Bridge Converter, with the load represented by a resistance R_{DC}.

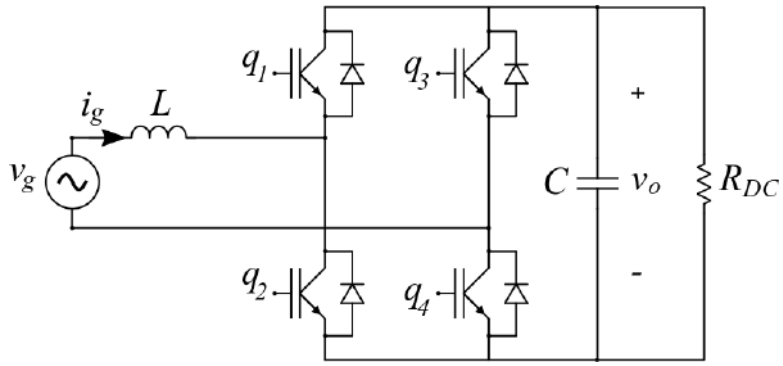


Figure 3.12: Model of Single-Phase Bidirectional Boost Rectifier.

The input-output voltage relationship in steady state is given by

$$\frac{V_o}{\bar{V}_g} = \frac{1}{1-2d}. \tag{3.26}$$

Substituting the resistor emulator law (3.20) in (3.26) it is obtained

$$R_s \bar{I}_g = V_m(1-2d). \tag{3.27}$$

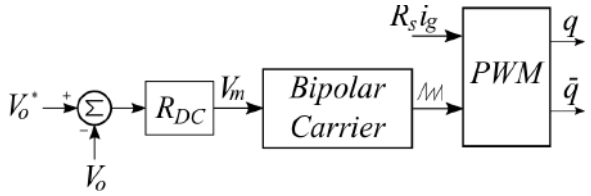
where $V_m = R_s V_o / R_e$.

The schematic of this strategy is depicted in Figure 3.13. The carrier amplitude V_m is defined by the DC-bus voltage regulator, and the right side of (3.27) is realized by a bipolar carrier, with its waveform described by $V_m(1 - t/(K_1 T_s)$, which for convenience K_1 is defined in [98] with a value of 0.5.

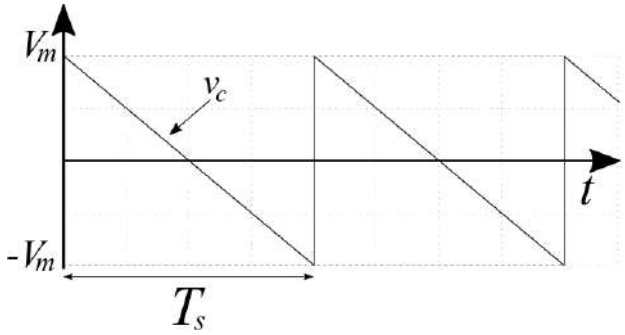
Making d explicit from (3.26)

$$d = 0.5\left(1 - \frac{\bar{V}_g}{V_o}\right). \tag{3.28}$$

Therefore, the current control is realized such that the duty-cycle d is modulated to follow v_g, and to keep the DC-link voltage at its reference value, since the DC bus is fed by the input current.



(a)



(b)

Figure 3.13: Bipolar OCC: (a) Schematic (b) Sawtooth Carrier Waveform.

The converter of Figure 3.12-(a) is controlled with the resistor emulator approach and the result is shown in Figure 3.14. The input current is approximately sinusoidal and in phase with the input voltage, therefore the resistor emulator approach is achieved.

3.3.3 Grid Connected Inverter

The model of a Single-Phase Grid Connected Inverter is shown in Figure 3.15 and it consists of a Single-Phase AC source v_g and a Full-Bridge Converter, with the DC-bus fed by a DC current i_{DC}.

In this case the converter emulates a negative resistance, $R_e < 0$ such that grid current flows from the converter to the grid.

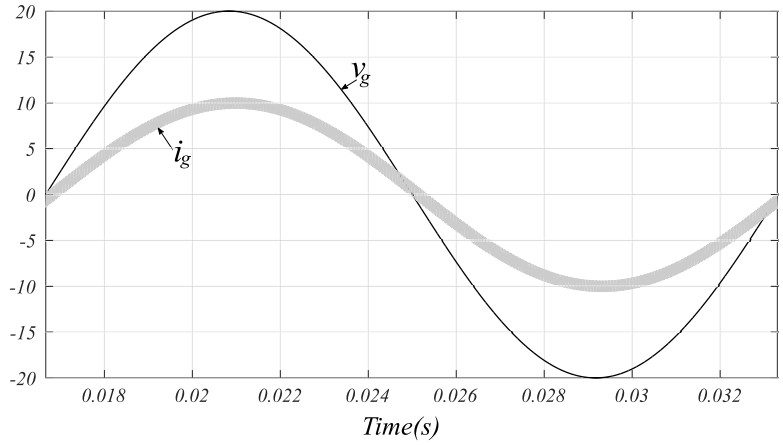


Figure 3.14: Single-Phase Bidirectional Boost Rectifier with OCC: Input Voltage (5 V/div.) and Input Current (1 A/div.).

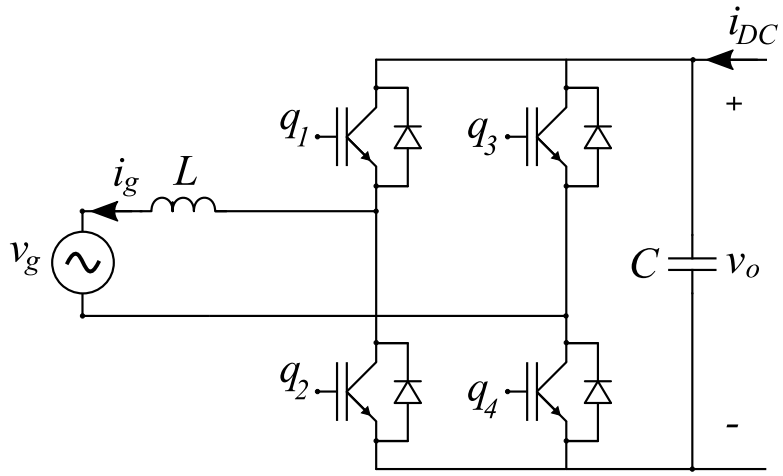


Figure 3.15: Model of Single-Phase Grid Connected Inverter.

The input-output voltage relationship in steady state is given by

$$\frac{V_o}{\bar{V_g}} = \frac{1}{1-2d}. \tag{3.29}$$

The classical approach of OCC for GCI demands the employment of grid voltage sensors [99]. The sensed voltage is further multiplied by a gain k, which has to do with maximum power flow and system convergence speed, and then subtracted from the sensed grid current and the resulting value is compared with the modulated carrier, as shown in Figure 3.16

The control law for this implementation is given by

$$kv_g + R_s\bar{I_g} = V_{ms}(1-2d), \tag{3.30}$$

where $V_{ms} = R_s V_o / R_{es}$.

In [100] it was proposed an OCC-based strategy for light load operation and GCI without grid voltage sensors, where the sensed voltage signals were replaced by an

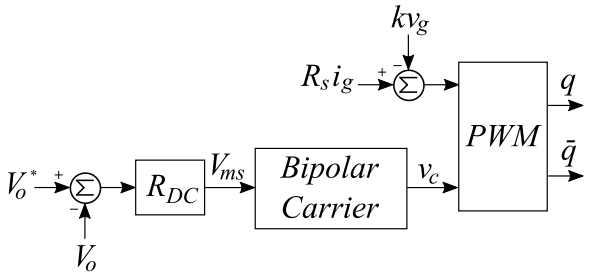


Figure 3.16: Block Diagram of OCC with Voltage Measurement for Single-Phase Grid Connected Inverter.

approximation calculated from available variables on the control. The duty-cycle d is reconstructed from the PWM output Q by a Second Order Low-Pass Filter and the voltage grid can be approximately calculated by3.26. The schematics is shown if Figure 3.17.

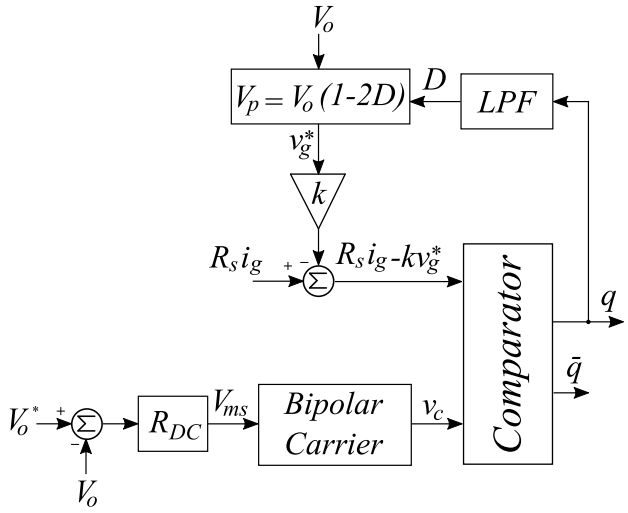


Figure 3.17: Block Diagram of OCC with no Voltage Measurement for Single-Phase Grid Connected Inverter.

Therefore considering the reconstructed grid voltage $\hat{v_g}$ the control becomes

$$kv_g^* + R_s\bar{I}_g = V_m(1-2d). \tag{3.31}$$

Making d explicit from (3.29)

$$d = 0.5\left(1 - \frac{v_g(t)}{V_o}\right). \tag{3.32}$$

The grid current control is realized such that the duty-cycle d is modulated to follow v_g, and to keep the DC-link voltage at its reference value, since the DC bus is fed by the input DC current i_{DC}.

The converter of Figure 3.17 is controlled with the approach of Negative Resistance Emulation with grid voltage measurement and the result is shown in Figure 3.18.

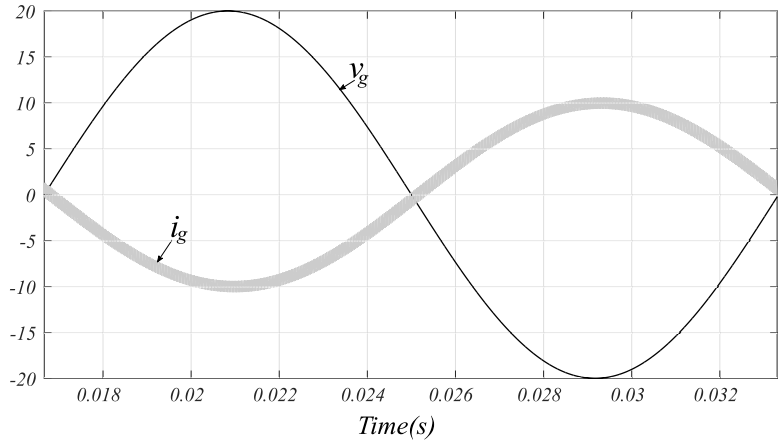


Figure 3.18: Grid Connected Inverter with OCC: Input Voltage (5 V/div.) and Input Current (1 A/div.).

3.4 Digital OCC

As seen in Chapter 1, digital devices are increasing more and more their role in control of converters. The flexibility of implementation is the main advantage of the use of these devices. Even though the OCC technique was proposed as an analog control technique, digital implementations for some OCC strategies can be derived.

The OCC technique has been digitally implemented in DSP for application in PFC [27] and APF [28] however the derivation of digital OCC strategies may have some challenges to be overcome.

From (3.16)-(3.30), making simple manipulation and disregarding R_s gives

$$\frac{\bar{I}_g}{V_m} = f(d), \tag{3.33}$$

and

$$\frac{\bar{I}_g + k\bar{V}_g}{V_{ms}} = f(d). \tag{3.34}$$

The right sides of (3.33)-(3.34) are realized by unitary amplitude carriers and, as seen in last section, the carriers may assume several waveforms such as linear, quadratic and paraboloid. By the other hand, common microprocessor-based devices usually have hardware linear carrier generators (sawtooth and triangular waveforms), therefore OCC strategies with non-linear carrier could not be implemented in these devices.

An alternative for implementing a non-linear carrier is a software generated carrier signal, which brings the drawback of bigger computational effort and a narrower bandwidth since the carrier value is updated at a digital clock-frequency-multiple time step. Another alternative is to develop dedicated analog circuits to generate the non-linear carrier, but that demands extra A/D and D/A converters, what increases

cost and volume of the application.

For linear carrier OCC strategies, therefore, (3.33)-(3.34) can be realized by comparation of a unitary-amplitude linear carrier with the sensed current (and grid voltage for some strategies) divided by the DC bus controller output V_m. This strategy is shown in Fig. 3.19.

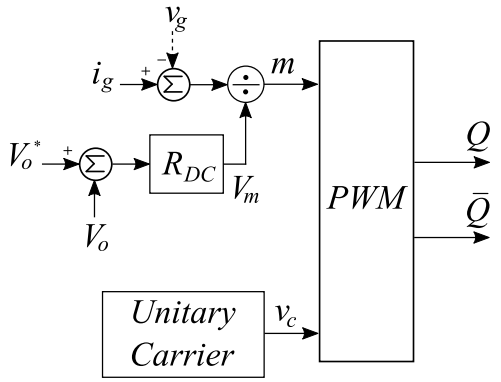


Figure 3.19: Block Diagram of DOCC Technique.

3.5 Three-Phase OCC

In this section, three analog OCC strategies for controlling three-phase three-leg boost converters which can be applied to PFC Rectifiers, APF and GCI are presented. The first strategy has the simplest implementation among all and it rests on the assumption of decoupling between phases. The second one is based on control with vector operation, having lower switching losses and improvements on utilization of DC-bus. The last strategy is based on Hybrid PWM, so that it inherits the advantages of first two strategies: simpler implementation from Bipolar OCC, and lower switching losses and better utilization of DC-bu from Vector-Based OCC.

Assume:

- x = a, b, c;
- d_{xp} and d_{xn} are the upper and lower switches duty cycles, respectively.

3.5.1 Bipolar OCC

In Figure 3.20 is shown the schematic of a Three-Phase Full-Bridge Converter Connected to a Three-Phase Grid, consisting of three legs, a DC bus with voltage V_o. On the AC side, the converter is connected to the grid through an inductance L_g in each phase. The grid is modeled as an ideal three phase AC source with phase voltages v_{gx}.

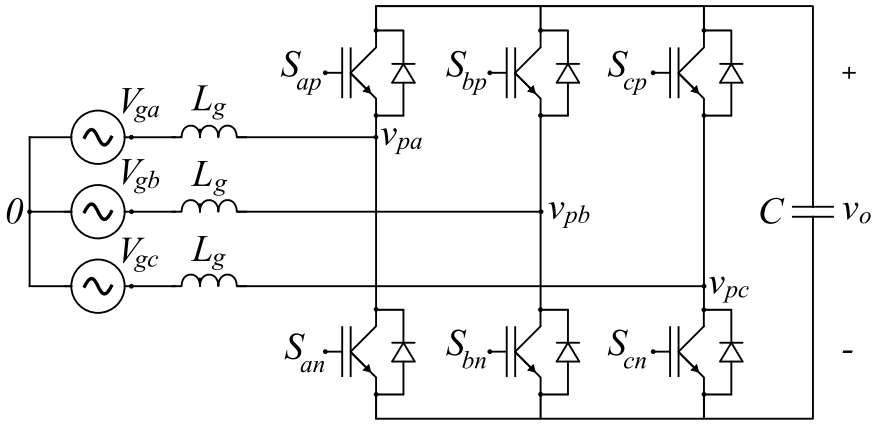


Figure 3.20: Three-Phase Full-Bridge Converter Connected to a Three-Phase Grid - General Model.

Based on the quasi-steady-state approach, the average model of the converter is a three-phase voltage controlled source with neutral point n as illustrated in Figure 3.21.

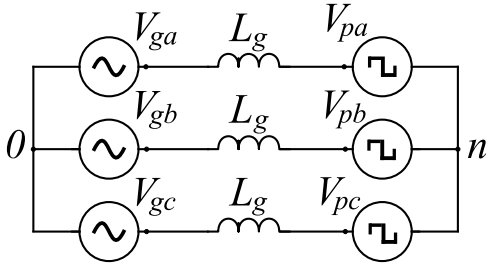


Figure 3.21: Two level three phase full bridge rectifier - Average Model.

The averaged pole voltages within one cycle V_{px} are related to the leg converter quasi-steady-state transfer function $f_p(d)$ such that

$$V_{px} = f_p(d)V_o. \tag{3.35}$$

Considering the bipolar carrier-based PWM modulation the control law becomes

$$V_{px} = (1 - 2d_{xn})V_o, \tag{3.36}$$

where $V_o = \frac{V_{DC}}{2}$.

The mesh equations for each phase can be written as:

$$v_{gx} = L_g \frac{d}{dt} i_{gx} + R_g i_{gx} + V_{px} + V_{n0}. \tag{3.37}$$

Writing it in matrix form

$$\begin{bmatrix} V_{ga} \\ V_{gb} \\ V_{gc} \end{bmatrix} = L_g \frac{d}{dt} \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} + \begin{bmatrix} V_{pa} \\ V_{pb} \\ V_{pc} \end{bmatrix} + \begin{bmatrix} V_{n0} \\ V_{n0} \\ V_{n0} \end{bmatrix}. \tag{3.38}$$

As seen earlier in this chapter, the inductive drop can be neglected. Therefore, for $L_g \approx 0$ (3.38) becomes

$$\begin{bmatrix} V_{ga} \\ V_{gb} \\ V_{gc} \end{bmatrix} = \begin{bmatrix} V_{pa} \\ V_{pb} \\ V_{pc} \end{bmatrix} + \begin{bmatrix} V_{n0} \\ V_{n0} \\ V_{n0} \end{bmatrix}. \tag{3.39}$$

Considering the system as symmetric

$$\begin{cases} v_{ga}(t) + v_{gb}(t) + v_{gc}(t) = 0 \\ i_{ga}(t) + i_{gb}(t) + i_{gc}(t) = 0 \end{cases}, \tag{3.40}$$

leads to

$$V_{n0} = -\frac{1}{3}(V_{pa} + V_{pb} + V_{pc}). \tag{3.41}$$

Replacing (3.41) into (3.39)

$$\begin{bmatrix} V_{ga} \\ V_{gb} \\ V_{gc} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} V_{pa} \\ V_{pb} \\ V_{pc} \end{bmatrix}. \tag{3.42}$$

Substituting (3.36) into (3.42) yields to the expression (3.43) and its shortened form (3.44), which relate the instantaneous duty cycle values of each converter arm and the values of the phase voltages.

$$\begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} 1 - 2d_{an} \\ 1 - 2d_{bn} \\ 1 - 2d_{cn} \end{bmatrix} = \frac{1}{V_o} \begin{bmatrix} V_{ga} \\ V_{gb} \\ V_{gc} \end{bmatrix}. \tag{3.43}$$

(3.43) can be rewritten in matrix form

$$T[1 - 2d_{xn}] = \frac{1}{V_o} V_{gx}. \tag{3.44}$$

The matrix T is singular, so that there is no single solution to the equation. A possible solution is presented in [99] as

$$\begin{bmatrix} d_{an} \\ d_{bn} \\ d_{cn} \end{bmatrix} = \begin{bmatrix} K_1 - \frac{1}{2}\frac{v_{ga}}{V_o} \\ K_1 - \frac{1}{2}\frac{v_{gb}}{V_o} \\ K_1 - \frac{1}{2}\frac{v_{gc}}{V_o} \end{bmatrix}, \tag{3.45}$$

where K_1 is an introduced parameter related to the voltage V_{N0}.

By replacing (3.45) in (3.43) the general relationship between the grid phase voltages and the voltages synthesized by the converter is then given by

$$\begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} = 2V_0K_1 \begin{bmatrix} 1 - \frac{d_{an}}{K_1} \\ 1 - \frac{d_{bn}}{K_1} \\ 1 - \frac{d_{cn}}{K_1} \end{bmatrix}. \tag{3.46}$$

Since the duty-cycles must be in the range [0, 1], and considering $m = \frac{\hat{V_g}}{V_o}$ it leads to

$$\frac{m}{2} \leq K_1 \leq 1 + \frac{m}{2}. \tag{3.47}$$

The goal of the PFC rectifier is to impose unitary PF, so the same methodology from Chapter 4 of resistance emulation is applied here

$$\begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} = R_e \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix}. \tag{3.48}$$

Then (3.45) becomes

$$\begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} = \frac{2V_oK_1}{R_e} \begin{bmatrix} 1 - \frac{d_{an}}{K_1} \\ 1 - \frac{d_{bn}}{K_1} \\ 1 - \frac{d_{cn}}{K_1} \end{bmatrix}. \tag{3.49}$$

Introducing the current output resistance R_s and defining V_m It turns to

$$R_s \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} = V_m \begin{bmatrix} 1 - \frac{d_{an}}{K_1} \\ 1 - \frac{d_{bn}}{K_1} \\ 1 - \frac{d_{cn}}{K_1} \end{bmatrix}. \tag{3.50}$$

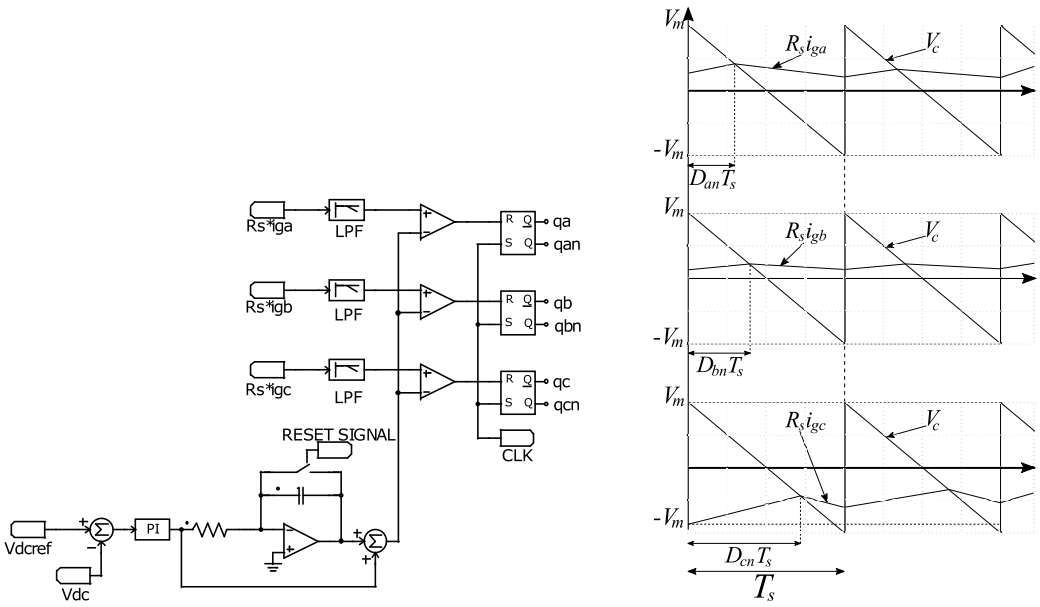
where $V_m = {}^{2R_sV_oK_1}/_{R_e}$ is the DC bus voltage controller output.

(3.50) describes the implementation of bipolar OCC and can be illustrated in Figure 3.22, where the representation of the analog implementation circuit and the operating waveforms of the method are shown. The currents are measured and compared to a periodic sawtooth wave generated by means of an integrator with periodic reset signal and a DC bus controller PI defining the carrier amplitude V_m.

3.5.2 Vector-Based OCC

In [4] it was proposed a modified implementation of OCC with lower switching losses by only two switches being controlled at switching frequency based on control with vector operation.

Since there are infinite solutions for (3.44), one possible solving choice is to set in each $60^{\underline{o}}$ line cycle the duty ratio of one of the switches to be zero or one, and



(a) (b)

Figure 3.22: Analog Implementation of OCC to three-phase Converter operating as PFC or APF: (a) Implementation Circuitry, (b) Waveforms.

the other two duty ratios to be controlled by the control law

$$R_s \begin{bmatrix} 2 & 1 \\ 1 & 2 \end{bmatrix} \begin{bmatrix} i_p \\ i_n \end{bmatrix} = V_m \begin{bmatrix} 1-d_p \\ 1-d_n \end{bmatrix}. \tag{3.51}$$

where i_p, i_n, d_p and d_n are the currents and duty ratios of the controlled phases, which are the input parameters to the control.

These input parameters are updated every $60^{\underline{o}}$ of line cycle, therefore this approach is similar space vector PWM [101]. The update approach is summarized in Table 3.2, which defines the duty cycles to be controlled and the switches driving signals based on the region where the voltage vector is located.

In Table 3.2 consider Q_{xp} and Q_{xn} the upper and lower switch driving signals, respectively.

Table 3.2: Vector-based OCC - Summarization of Input Control Parameters According to Line Cycle Region [4].

Region	i_p	i_n	d_p	d_n	Q_{an}	Q_{bn}	Q_{cn}
$0^{\underline{o}}$∼$60^{\underline{o}}$	i_a	i_c	d_{an}	d_{cn}	Q_p	ON	Q_n
$60^{\underline{o}}$∼$120^{\underline{o}}$	-i_b	-i_c	d_{bp}	d_{cp}	OFF	Q_p	Q_n
$120^{\underline{o}}$∼$180^{\underline{o}}$	i_b	i_a	d_{bn}	d_{an}	Q_n	Q_p	ON
$180^{\underline{o}}$∼$240^{\underline{o}}$	-i_c	-i_a	d_{cp}	d_{ap}	Q_n	OFF	$\bar{Q}_p$
$240^{\underline{o}}$∼$300^{\underline{o}}$	i_c	i_b	d_{cn}	d_{bn}	ON	Q_n	Q_p
$300^{\underline{o}}$∼$360^{\underline{o}}$	-i_a	-i_b	d_{ap}	d_{bp}	$\bar{Q}_p$	$\bar{Q}_n$	OFF

In Figure 3.23 is shown the control schematics for this approach. The Region

Selection block receives the sensed voltage signals and detects the region where the input voltage vector is located. The Input Current Selection block consists of a multiplexer circuit which receives this information and the sensed phase currents, and based on Table 3.2 determines the currents i_p and i_n to be controlled by OCC technique with control law (3.51), generating the driving signals Q_p, $\bar{Q}_p$, Q_n and $\bar{Q}_n$. With these signals and the information of which region the voltage vector is located, the Output Logic block defines switches driving signals Q_{xp} and Q_{xn} based on Table 3.2.

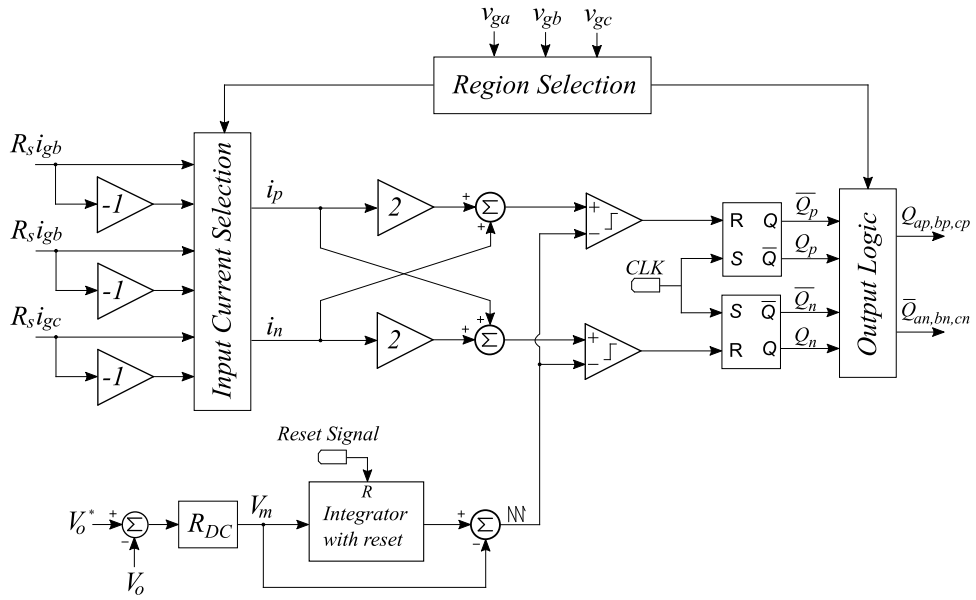


Figure 3.23: Control Schematics for OCC with Vector Operation.

Since the switches of only two legs are switched in each cycle, the switching are reduced by 33%. On the other hand, a drawback of this approach is the use of voltage measurements.

In [5] it is proposed a generalized vector-based OCC strategy for two level converters which considers the so called zero vector apportion ratio $0 \geq \mu \geq 1$. This introduced parameter defines the duration of realization of the null vectors in a switching cycle, what ultimately have influence on converter output voltage synthesis and switching losses.

Three special cases for μ are highlighted:

- $\mu = 0.5$: equal duration of the null vectors V7 e V0, bringing lower harmonics and equivalent switching losses;
- $\mu = 1.0$: realization of only null vector V7, bringing lower switching losses but with increased harmonics content;
- $\mu = 0.0$: realization of only null vector V0, with lower switching losses but with increased harmonics content.

Furthermore, it is shown that μ is related to the common mode voltage V_{N0} by the relationship

$$V_{N0} = \frac{V_0}{2} - v_{max} - \mu(V_0 + v_{min} - v_{max}). \tag{3.52}$$

Since V_{N0} is a degree of freedom in (3.39), the common mode voltage can be chose according to μ.

The control schematic is shown in Figure 3.24 and is based on control law

$$R_s \begin{bmatrix} 2 & 1 & 0 \\ 0 & 3 & 0 \\ 0 & 1 & 2 \end{bmatrix} \begin{bmatrix} i_H \\ i_M \\ i_L \end{bmatrix} = V_m \begin{bmatrix} 1 - d_H \\ 1 - d_M \\ 1 - d_L \end{bmatrix}. \tag{3.53}$$

where i_H, i_M, i_L, d_H, d_M and d_L are the currents and duty ratios of the phases of maximum, intermediate and minimum values, respectively.

For the case with $\mu = 0.5$ this strategy can also be implemented in a digital approach

$$\frac{R_s}{V_m} \begin{bmatrix} 2 & 1 & 0 \\ 0 & 3 & 0 \\ 0 & 1 & 2 \end{bmatrix} \begin{bmatrix} i_H \\ i_M \\ i_L \end{bmatrix} = \begin{bmatrix} 1 - d_H \\ 1 - d_M \\ 1 - d_L \end{bmatrix}. \tag{3.54}$$

In Figure 3.24 is depicted the control schematics for this strategy. The Region Selection receives the average values of grid currents and a reference value of μ, defining the signals for selection for input currents and output logic for the switching signals, besides the value of μ to the control.

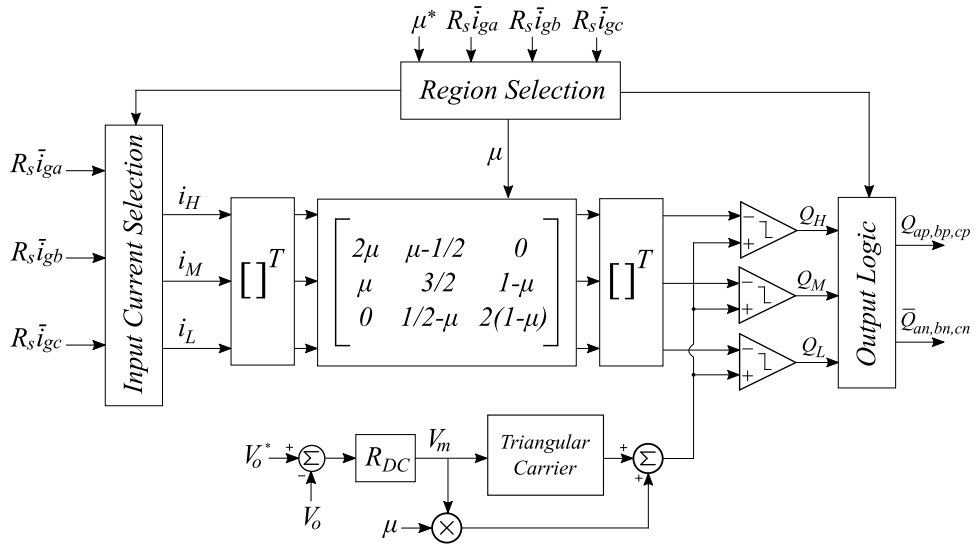


Figure 3.24: Control Schematics for Generalized Analog Vector-Based OCC for Two Level Converters with μ.

The realization map of the combinational logic circuits for this strategy for the

Input Current Selecion Block and Output Logic Block is summarized in Table 3.3.

Table 3.3: Generalized Vector-based OCC - Summarization of Input Control Parameters According to Line Cycle Region [5].

Region	i_H	i_M	i_L	Q_{an}	Q_{bn}	Q_{cn}
$0^{\underline{o}}$∼$60^{\underline{o}}$	i_c	i_a	i_b	Q_M	Q_L	Q_H
$60^{\underline{o}}$∼$120^{\underline{o}}$	i_a	i_c	i_b	Q_H	Q_L	Q_M
$120^{\underline{o}}$∼$180^{\underline{o}}$	i_a	i_b	i_c	Q_H	Q_M	Q_L
$180^{\underline{o}}$∼$240^{\underline{o}}$	i_b	i_a	i_c	Q_M	Q_H	Q_L
$240^{\underline{o}}$∼$300^{\underline{o}}$	i_b	i_c	i_a	Q_L	Q_H	Q_M
$300^{\underline{o}}$∼$360^{\underline{o}}$	i_c	i_b	i_a	Q_L	Q_M	Q_H

3.5.3 OCC with Hybrid PWM

Since OCC methods are fundamentally carrier-based techniques [102], the Hybrid PWM (HPWM) technique which correlates Carrier-Based PWM (CBPWM) and Space Vector PWM (SVPWM) methods [103] to take advantages of simplicity of implementation from CBPWM and enhanced performance on output voltage synthesis and DC-bus utilization from SVPWM [104] can be applied the OCC for three-phase converters. The HPWM is based on the injection of an appropriate zero sequence component into the modulating signals [105] to obtain results identical to SVPWM.

In [5] it is proposed a generalized HPWM OCC strategy for two level converters which considers the the parameter μ to have results similar to those with vector-based approach but with simpler implementation.

The control is described by control law

$$R_s \begin{bmatrix} i_H \\ i_M \\ i_L \end{bmatrix} + R_s \begin{bmatrix} i_{N0} \\ i_{N0} \\ i_{N0} \end{bmatrix} = V_m \begin{bmatrix} 1-d_H \\ 1-d_M \\ 1-d_L \end{bmatrix}, \tag{3.55}$$

where i_{N0} is the common-mode current given by

$$i_{N0} = \frac{V_m}{2} - \mu(V_m + i_{min} - i_{max}). \tag{3.56}$$

The control scheme is shown in Figure 3.25, where the calculated commo- mode current is added to each sensed current and compared to the modulated linear carrier to generate the switching signals for the converter.

Further, this strategy can be modified to simplify the implementation circuit by substituting three adders by only one. This is done from manipulation of (3.55)

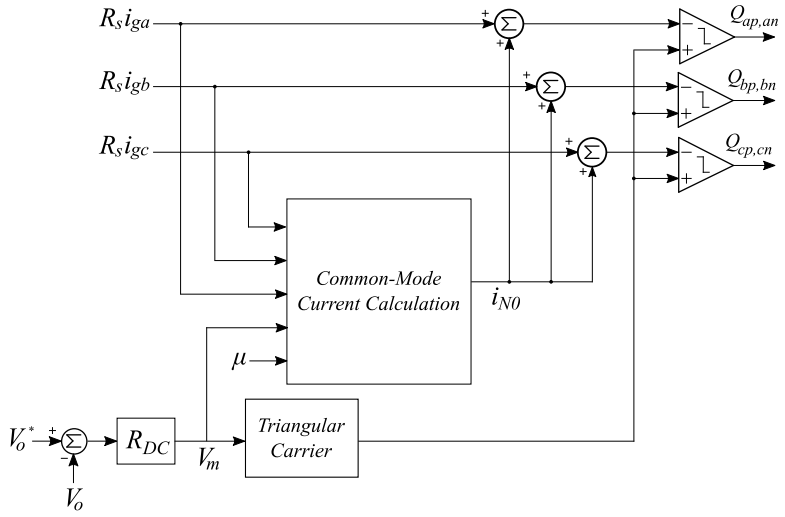


Figure 3.25: Control Schematics for Generalized Analog Hybrid PWM OCC with Linear Carrier.

$$R_s \begin{bmatrix} i_H \\ i_M \\ i_L \end{bmatrix} = V_m \begin{bmatrix} 1-d_H \\ 1-d_M \\ 1-d_L \end{bmatrix} - R_s \begin{bmatrix} i_{N0} \\ i_{N0} \\ i_{N0} \end{bmatrix}. \tag{3.57}$$

Observe that the right side of (3.53) is a modified carrier define by the sum of the linear carrier with amplitude V_m and the common mode current $R_s i_{N0}$.

The control scheme for this strategy is shown in Figure 3.26.

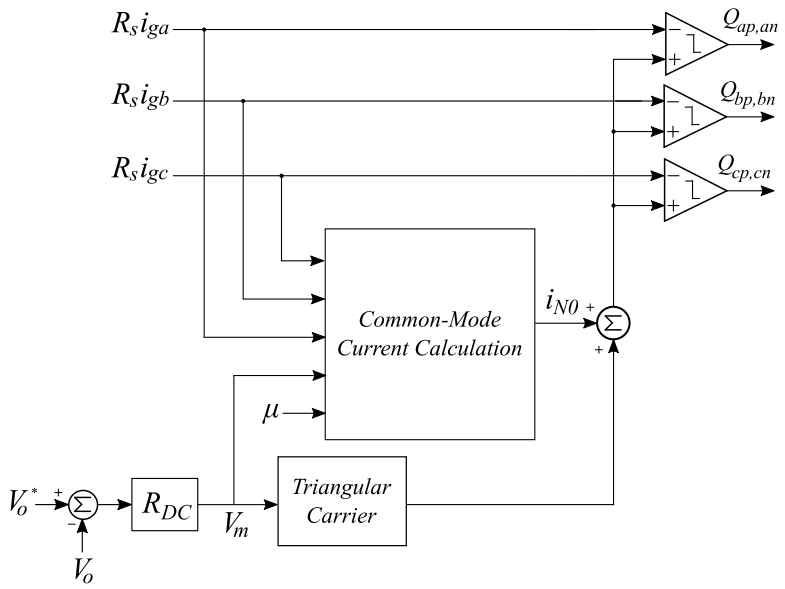


Figure 3.26: Control Schematics for Generalized Analog Hybrid PWM OCC with Non-Linear Carrier.

Modulation signals are shown in Figure 3.27 for generalized analog hybrid PWM OCC with Linear and Non-Linear Carriers for three values of μ. Observe that the modulations for the same value of μ the modulation with Linear and Non-Linear

carrier are equivalent.

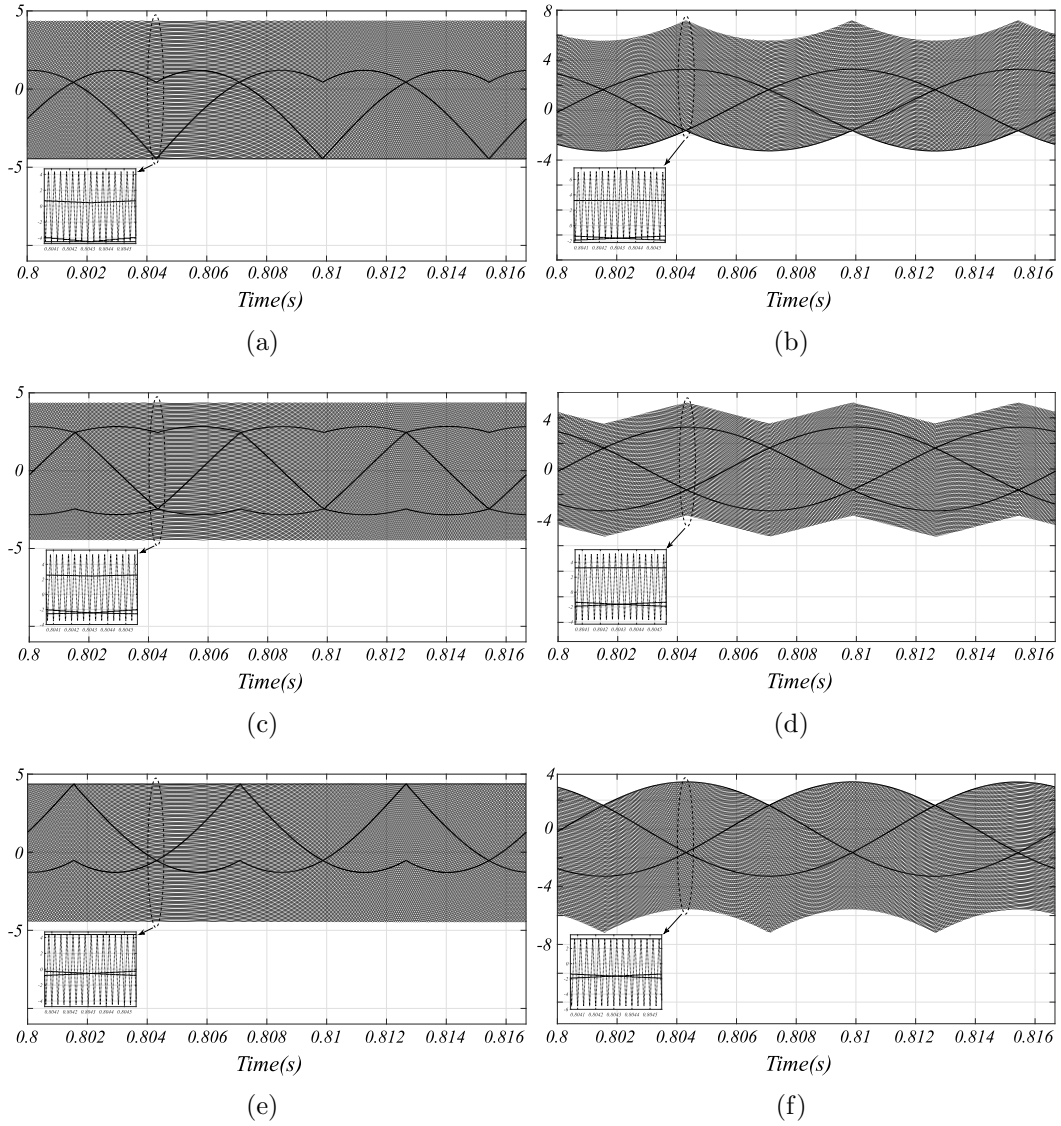


Figure 3.27: Modulation Signals for Generalized Analog Hybrid PWM OCC. Right Column - Linear Carrier: (a) $\mu = 0$, (c) $\mu = 0.5$, (e) $\mu = 1.0$. Left Column - Non-Linear Carrier: (b) $\mu = 0$, (d) $\mu = 0.5$, (f) $\mu = 1.0$.

3.5.4 PFC Rectifier

In Figure 3.28 it is shown the schematic of a two level three phase full bridge rectifier, which model consists of a three-phase full bridge converter with the DC side load represented by a resistance R_{DC}, with a OCC-based controller Block.

The sensed grid currents signals are inputs for the Control and Modulation block, which receives as well the sense DC-bus voltage signal, and additionally the sensed grid voltage signals for some OCC strategies.

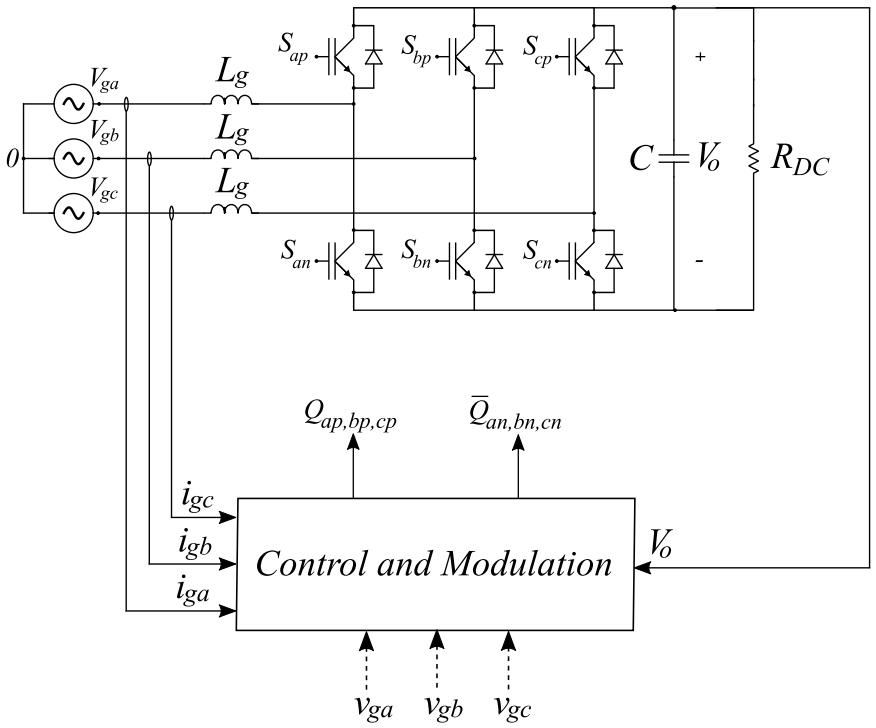


Figure 3.28: Three-Phase Full-Bridge PFC Rectifier - General Model.

3.5.5 Shunt APF

The APF controlled by OCC is shown in Figure 3.29. A very distinctive characteristic of this technique ii the fact that the current sensors are placed upstream to the PCC, so there is no need for measurement of load currents nor converter currents. This can be seen as an advantage, since the system cost and complexity is lower compared to those which demand load and converter currents measurements. However, since the controller currents are not controlled directly, the protection of the converter is degraded.

The goal of APF is similar to that of PFC rectifier, i.e., it aims to impose unitary PF on current grid so that

$$\begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} = \frac{1}{R_e} \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix}. \tag{3.58}$$

Applying Kirchhoff's current law on the circuit of Figure 3.29 the currents drawn by the converter are given by

$$\begin{bmatrix} i_{ca} \\ i_{cb} \\ i_{cc} \end{bmatrix} = \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} - \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix}. \tag{3.59}$$

If converter currents are such that they have reactive and harmonics content

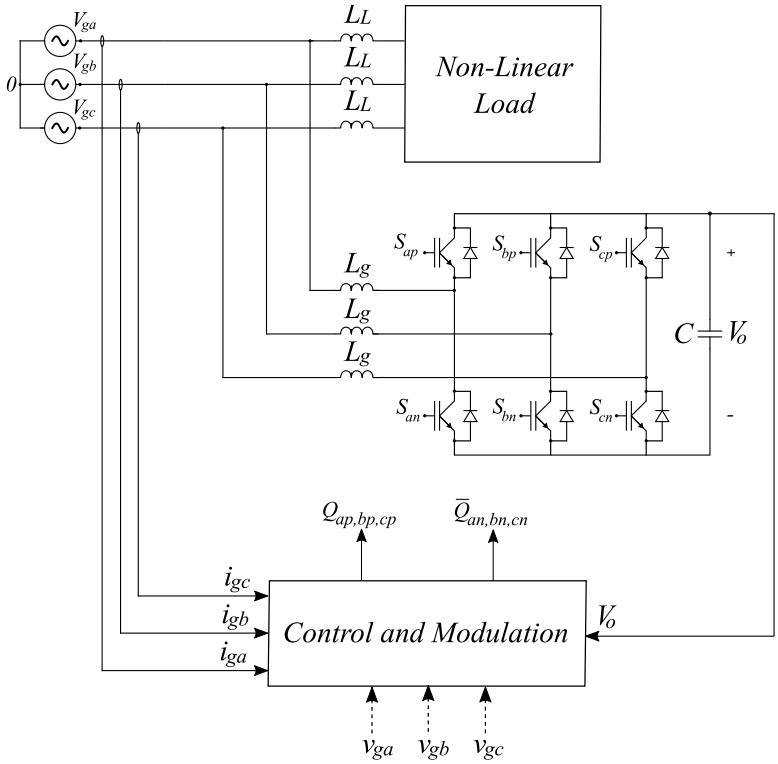


Figure 3.29: Three-Phase Full-Bridge Shunt APF - General Model.

with same amplitude and opposite phase of load currents, the whole harmonics and reactive content will be be drawn from the converter, leaving the grid to provide only active power.

From (3.50), the implementation equation for APF controlled by OCC is

$$R_s \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} = V_m \begin{bmatrix} 1-2d_{an} \\ 1-2d_{bn} \\ 1-2d_{cn} \end{bmatrix}, \tag{3.60}$$

where i_{ga}, i_{gb}, i_{gc} are the current measured upstream to the PCC, V_m is the output of DC bus voltage controller.

3.6 Feedforward Inductive Voltage Drop Compensation

In the analyzes done so far, the converter output inductance L has been neglected, so that the converter pole voltage v_p is considered equal to grid voltage v_g. This approximation is valid for DC-DC conversion and for AC-DC and DC-AC conversions with light load. However, for heavy load the influence of L is bigger and may lead to inaccurate results considering constraints with PF.

Consider the equivalent RL circuit in Figure 3.30.

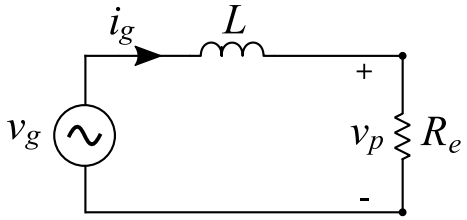


Figure 3.30: Equivalent RL Circuit for Converter with OCC with Resistor Emulator Approach.

Its phasor representation is given by

$$\mathbf{V_g} = R_e\mathbf{I_g} + j\omega L\mathbf{I_g}, \tag{3.61}$$

where $\mathbf{V_g}$ and $\mathbf{I_g}$ are the phasors of the fundamental component of grid voltage and grid current respectively.

The grid "sees" a RL load instead of a pure resistive load. Therefore a time constant τ_0 can be defined

$$\tau_0 = \frac{L}{R_e}. \tag{3.62}$$

The phasor diagram referring to (3.61) is shown in Figure 3.31. Observe that the grid current in classical OCC is always in phase with the converter fundamental component voltage.

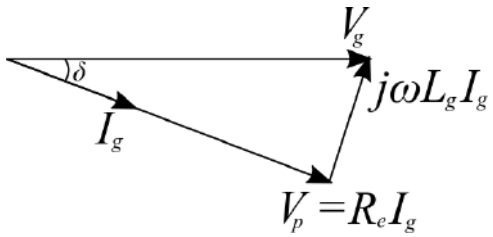


Figure 3.31: Phasor Diagram of Equivalent RL circuit of Single-Phase Bidirectional Rectifier controlled by OCC with Resistor Emulator Approach.

Therefore the grid current lags grid voltage by

$$\phi = \tan^{-1}\left(\frac{\omega L}{R_e}\right), \tag{3.63}$$

i.e., the bigger the load the bigger the displacement angle.

In [2] it was proposed a novel method to compensate phase lag in OCC-controlled rectifiers, which estimates the inductive voltage drop based on system parameters and on the estimation of the quadrature current.

In this strategy, instead of emulating a pure resistive load, the convert will emulate a RC load such that

$$\mathbf{V_{p1}} = \mathbf{Z_e I_g} = \left(R_e - j\frac{1}{\omega C_e}\right)\mathbf{I_g}. \tag{3.64}$$

Applying to (4.42) leads to

$$\mathbf{V_g} = \Big(R_e - j\frac{1}{\omega C_e}\Big)\mathbf{I_g} + j\omega L\mathbf{I_g}. \tag{3.65}$$

Making

$$C_e = \frac{1}{\omega^2 L}. \tag{3.66}$$

leads to

$$\mathbf{V_g} = R_e\mathbf{I_g}. \tag{3.67}$$

Therefore the grid current becomes in phase with the grid voltage.

From (3.64) the OCC strategy can be derived and considering the sensor current ouput resistance R_s

$$R_s I_g - jK_c I_g = V_m(1-2d). \tag{3.68}$$

where $K_c = {}^{\omega LR_s}/_{R_e}$ is the quadrature current compensation gain.

The second term of the left side is the inductive voltage drop to be compensated and it is estimated from the quadrature current calculated by the $90^{\underline{o}}$ Phase Lag Shifter and the quadrature current compensation gain K_c.

The control schematics of the strategy with feedforward inductive voltage drop compensation is shown in Figure 3.32-a with digital implementation. The voltage drop is estimated from the quadrature current calculated by the $90^{\underline{o}}$ Phase Lag Shifter, which consists of two second-order LPF followed by a gain of -2 as illustrated in Figure 3.32-b. Then the quadrature current is further multiplied by a dynamic gain from system variables and parameters to calculate the inductive voltage drop, which is summed to the measured current and the result divided by the output of the DC-bus controller, to do the usual digital OCC modulation.

The transfer function of the $90^{\underline{o}}$ Phase Lag Shifter is given by

$$H_f(s) = -2\Big(\frac{\omega_c^2}{s^2 + 2\xi\omega_c s + \omega_c^2}\Big)\Big(\frac{\omega_c^2}{s^2 + 2\xi\omega_c s + \omega_c^2}\Big), \tag{3.69}$$

which results in a 4th order transfer function.

The new equivalent circuit and its Phasor Diagram are depicted in Figure 3.33. The converter pole voltage leads the grid voltage by $\delta = -atan(1/(\omega C_e R_e))$ so that phase current is in phase with phase voltage.

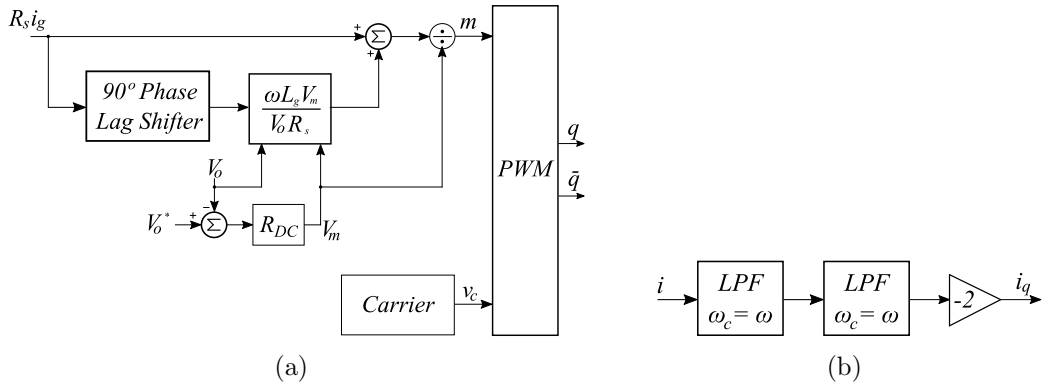


Figure 3.32: Feed-Forward Inductive Voltage Drop Compensation: (a) General Block Diagram, (b) Block Diagram of the 90^o Phase Lag Shifter - Adapted from [2].

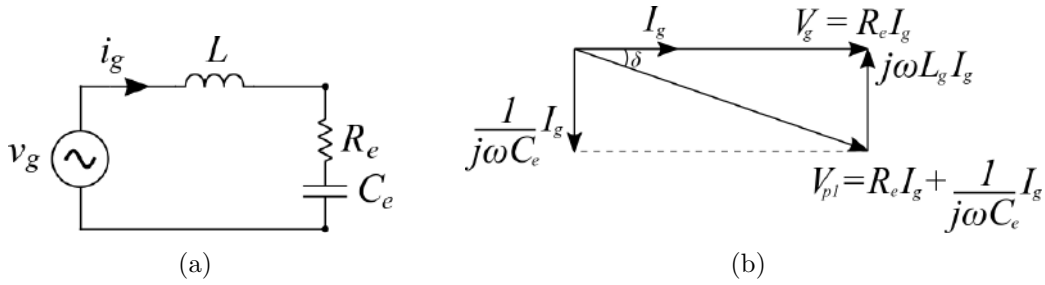


Figure 3.33: Feed-Forward Inductive Voltage Drop Compensation: (a) RLC Equivalent circuit, (b) Phasor Diagram with Inductive Voltage Drop Compensation.

3.7 Partial Conclusions

In this Chapter it was presented a general review on OCC, with its main aspects, starting from the general theory of this analog technique and the implementation of OCC with Resistor Emulator approach, which can be used to control converters to achieve almost unitary PF and low harmonics content. The digital implementation of linear-carrier OCC were also reviewed, presenting the equivalence between analog and digital forms. For three-phase converters, the bipolar-based and vector-based OCC strategies were also presented. Finally, the inherent inductive voltage drop, which can deteriorate PF for heavy load, was also presented, together with the solution found in literature for this problem.

Chapter 4

Contributions and Discussion

4.1 Introduction

In this Chapter some contributions for Analog and Digital OCC are presented. A general approach for the use of grid voltage measurements in OCC for PFC rectifiers, APF and GCI is proposed, defining their application and limits. Also, the stability analysis for OCC technique with triangular carrier is done for through Poincaré Maps, defining the mandatory inductance for the convergence of duty-cycle. The small-signal analyzes for Analog and Digital OCC are done. Further, it is proposed a modification on the strategy to compensate the inductive voltage drop, with use of a different 90^{o} phase shifter. Finally, the HPWM is extended to DOCC.

4.2 Influence of Carrier Waveform on Stability of OCC Technique

The stability analysis of control methods can be analyzed using the Poincaré Maps, which is an effective approach for analyzing the dynamics and stability of non-linear systems [106]. In [107] it is studied the stability for the convergence of duty cycle of converters with non-linear control with sawtooth carrier. It results in a mandatory inductance value for system stability

$$L > \frac{1}{2f_s}\frac{V_g}{I_{gmin}} = L_{minSAW}. \tag{4.1}$$

The PWM block can also be done with a triangular carrier [26]. The employment of triangular carrier allows to remove the flip-flop and the clock generator and avoids the need for averaging schemes for the sensed line current.

The stability analysis for the convergence of duty cycle for converters controlled by OCC with triangular carrier is not found in literature. This is going to be carried

out in this section. First the concept of Poincaré Maps is introduced, together with the duty cycle convergence ratio λ. Then this approach is applied to derive the minimum inductance for duty cycle convergence of OCC with triangular carrier.

4.2.1 Poincaré Maps

A generic n-order continuous-time dynamic system governed by the differential equation

$$\frac{d}{dt}x = f(t, x), \tag{4.2}$$

where x(t) is the n-dimensional state vector in function of the independent variable time t.

The value x_T at time $t = T$ is obtained by means of integration of function $f(.)$ within a period T starting from an initial value x_0 at time $t = 0$, therefore

$$x_T = \int_0^T f(\tau, x(\tau))\,\mathrm{d}\tau + x_0. \tag{4.3}$$

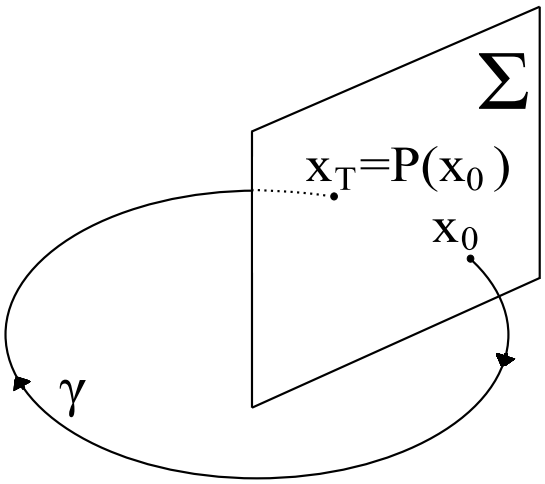


Figure 4.1: Poincaré Map and Boundary Value Condition - Adapted from [3].

The dynamic behavior of an unidimentional system can be described by the Poincaré Map shown in Figure 4.1, where x_0 starts from Poincaré Section $\sum$ at $t = 0$ and returns to the Section to point x_T at $t = T$ by the closed path γ. $\mathbf{P}(.)$ is a mapping relationship from x_0 to x_T and normally is nonlinear to x_0 such that

$$x_T = \mathbf{P}(x_0). \tag{4.4}$$

For steady-state operation the values x_0 and x_T are equal, i.e.

$$x^* = \mathbf{P}(x_0) = x_0. \tag{4.5}$$

The point x^* is called fixed point, since its value is not modified by the mapping $\mathbf{P}(.)$. If for any x_0 the sequence converges to $x = x^*$ this point is called attracting fixed point, on the other hand, if the sequence diverges the fixed point is called non-attracting. A attracting fixed point of a mapping relationship corresponds to a steady-state stable point of a continuous time system [108].

It is possible to analyze the stability of a system by means of the mapping relationship $\mathbf{P}(.)$ [109]. For a n-order system the condition for stability of fixed points is that the eigenvalues of the Jacobian Matrix of $\mathbf{P}(.)$ are placed inside the unitary cycle. For example, for a first order system:

$$\left|\lambda = \frac{\partial}{\partial x_0}\mathbf{P}(x_n)\right| < 1. \tag{4.6}$$

For an unidimensional system, the mapping relationship can written in the form (4.7)

$$\mathbf{P}(x_n) = (1 - \lambda^n)x^* + \lambda^n x_0. \tag{4.7}$$

For a convergent mapping, i.e., $|\lambda| < 1$, there exists three distinct cases for which examples of duty-cycle convergence are presented in Figure 4.2:

- $-1 < \lambda < 0$ the convergence to x^* occurs in a oscillatory manner;
- $\lambda = 0$ the convergence to x^* occurs in one period T;
- $0 < \lambda < 1$ the converges to x^* monotonically increasing.

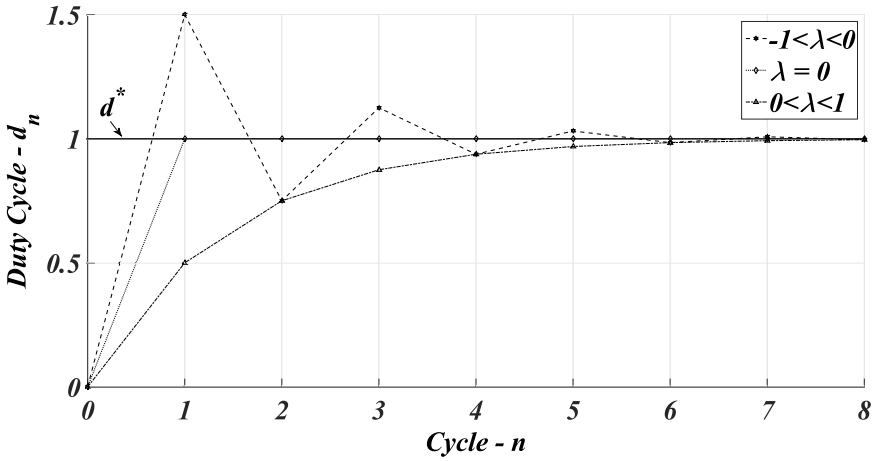


Figure 4.2: Duty-Cycle Convergence of Convergent Mapping Systems.

4.2.2 One-cycle Control with Triangular Carrier

In Figure 4.3 It is shown the schematics of a CC-CC bidirectional boost converter.

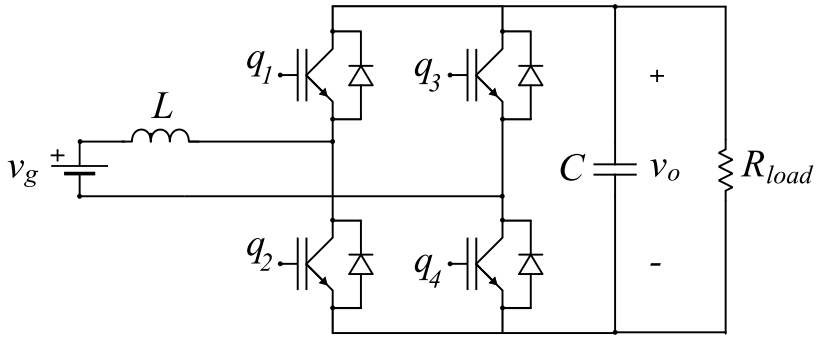


Figure 4.3: Model of DC-DC Full-Bridge Boost Converter.

The converter is controlled by an OCC-based control technique. The evolution of the modulating signal v_i, the triangular carrier v_c and duty cycle d_n of switches q_2 and q_3 during a transient are shown in Figure 4.4. The inductor current rising slope m_1 and falling slope m_2, and the carrier rising and falling slope m_c are given by (4.8).

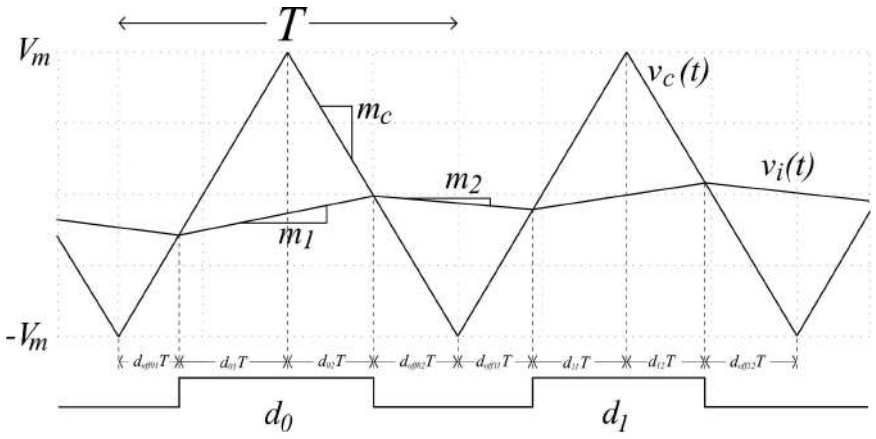


Figure 4.4: DC-DC Full-Bridge Boost Converter with OCC - Waveforms of Measured Current and Triangular Carrier During Transient.

$$\begin{cases} m_1 = \frac{|v_g + V_0|}{L}; \\ m_2 = \frac{|v_g - V_0|}{L}; \\ m_c = 4V_m f_s. \end{cases} \tag{4.8}$$

From the analysis of Figure 4.5 and equaling the vertical distances between point at the beginning of the period ($V_c = -V_m$) and the point of minimum value of current, between the points of minimum and maximum of current signal, and between the point of maximum value of current and the point at the end of the period ($V_c = -V_m$) one gets

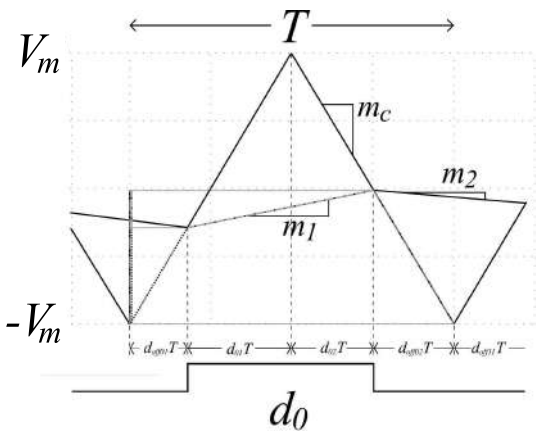


Figure 4.5: DC-DC Full-Bridge Boost Converter with OCC - Waveforms of First Equalizing Path of Measured Current and Triangular Carrier During Transient.

$$m_c d_{off01} T + m_1 d_0 T = m_c d_{off02} T. \tag{4.9}$$

Observe that

- $d_{off01} = \big(1/2 - d_{01}\big)$;
- $d_{off02} = \big(1/2 - d_{02}\big)$;
- $d_0 = (d_{01} + d_{02})$.

Therefore (4.9) becomes

$$m_c\big(1/2 - d_{01}\big)T + m_1\big(d_{01} + d_{02}\big)T = m_c\big(1/2 - d_{02}\big)T. \tag{4.10}$$

Rearranging one obtains

$$d_{01}(m_c - m_1) = d_{02}(m_1 + m_c). \tag{4.11}$$

Summing up $d_{01}(m_1 + m_c)$

$$d_{01}(2m_c) = (d_{01} + d_{02})(m_1 + m_c) = d_0(m_1 + m_c). \tag{4.12}$$

Hence

$$d_{01} = \frac{m_c + m_1}{2m_c} d_0. \tag{4.13}$$

By similar procedure

$$d_{02} = \frac{m_c - m_1}{2m_c} d_0. \tag{4.14}$$

For the second cycle by analogous approach the relationships for duty cicles can be obtained

$$d_{11} = \frac{m_c + m_1}{2m_c} d_1. \tag{4.15}$$

$$d_{12} = \frac{m_c - m_1}{2m_c} d_1. \tag{4.16}$$

From Figure 4.6, equaling the path from the peak of the carrier in the first cycle ($v_c = V_m$) and the point of maximum value of current in the first period (red path), the path the point of maximum value of current in the first period and the minimum value of current in the second period, the path from the minimum current in the second period and the maximum current value in second period and finally the path from the maximum current value in second period and the peak of the carrier in the second cycle one obtains

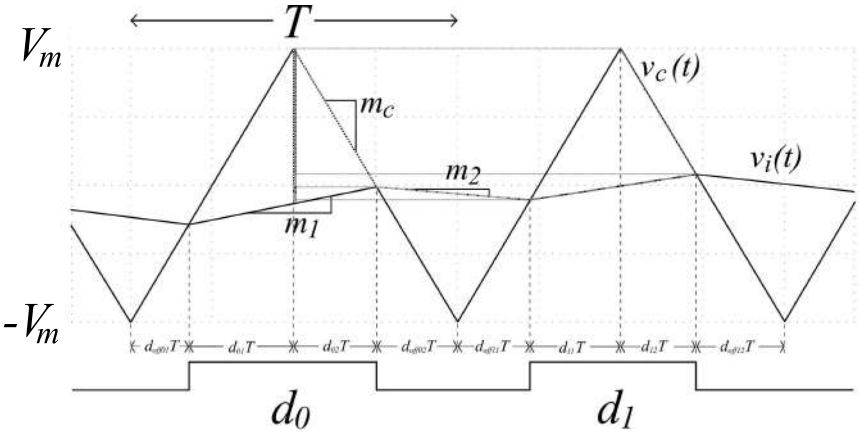


Figure 4.6: DC-DC Full-Bridge Boost Converter with OCC - Waveforms of Second Equalizing Path of Measured Current and Triangular Carrier During Transient.

$$m_c d_{02} T + m_2(d_{off02} + d_{off11})T = m1 d_1 T + m_c d_{12} T. \tag{4.17}$$

Becoming

$$m_c d_{02} + m_2(1/2 - d_{02} + 1/2 - d_{11}) = m_1(d_{11} + d_{12}) + m_c d_{12}. \tag{4.18}$$

In its turn

$$d_{12}(m_c + m_1) + d_{11}(m_1 + m_2) + d_{02}(m_2 - m_c) - m_2 = 0. \tag{4.19}$$

Replacing (4.14),(4.15) and (4.16) in (4.19)

$$\frac{(m_c - m_1)(m_c + m_1)}{2m_c} d_1 + \frac{(m_c + m_1)(m_1 + m_2)}{2m_c} d_1 + \frac{(m_c - m_1)(m_2 - m_c)}{2m_c} d_0 - m_2 = 0. \tag{4.20}$$

The relationship that maps the cycle d_1 from d_0 is derived

$$d_1 = \frac{2m_2m_c}{(m_1+m_c)(m_2+m_c)} + \frac{(m_1-m_c)(m_2-m_c)}{(m_1+m_c)(m_2+m_c)}d_0. \tag{4.21}$$

The equilibrium point is obtained from $f(d^*) = d^*$

$$\hat{d} = \frac{2m_2m_c}{(m_1+m_c)(m_2+m_c)} + \frac{(m_1-m_c)(m_2-m_c)}{(m_1+m_c)(m_2+m_c)}\hat{d}.$$

Thence

$$\hat{d} = \frac{m_2}{m_1+m_2} = \frac{v_g}{V_0}.$$

Defining λ the duty-cycle convergence ratio by

$$\lambda = \frac{\partial}{\partial d_n}\mathbf{P}(d_n) = \frac{(m_1-m_c)(m_2-m_c)}{(m_1+m_c)(m_2+m_c)}. \tag{4.22}$$

The mapping function $\mathbf{P}()$ can be written in the form

$$d_{n+1} = \mathbf{P}(d_n) = (1-\lambda^n)\hat{d} + \lambda^n d_n.$$

Considering the stability criterion $|\lambda| < 1$

$$-1 < \frac{(m_1-m_c)(m_2-m_c)}{(m_1+m_c)(m_2+m_c)} < 1. \tag{4.23}$$

Solving

$$\begin{cases} (m_c)^2 + m_1m_2 > 0; \\ m_c(m_1+m_2) > 0. \end{cases} \tag{4.24}$$

From (4.8), since the values of m_c, m_1, m_2 are always positive, (4.24) would conduce to a stable system for any L and f_s. However, as it going to be seen in this section, there will be minimum f_s and L for duty cycle convergence due to physical limitations of the switching devices.

First, considering the converter from Figure 4.3 with $v_g = 100,0$V, $v_0 = 200,0$V e $R_{DC} = 40{,}0\ \Omega$. The output of the DC bus controller is

$$V_m = \frac{V_0}{R_e} = 20. \tag{4.25}$$

The behavior of λ according to varations in L and f_s are shown in Figure 4.7 for $f_s = 30$ kHz and Figure 4.8 - for L = 550,0 λH. It can be defined three different regions of convergence:

$$\begin{cases} I: \ m_1 < m_c \text{ e } m_2 \leq m_c, \ \lambda \geq 0; \\ II: \ m_1 > m_c \text{ e } m_2 < m_c, \ \lambda < 0; \\ III: \ m_1 \leq m_c \text{ e } m_2 > m_c, \ \lambda \geq 0. \end{cases} \tag{4.26}$$

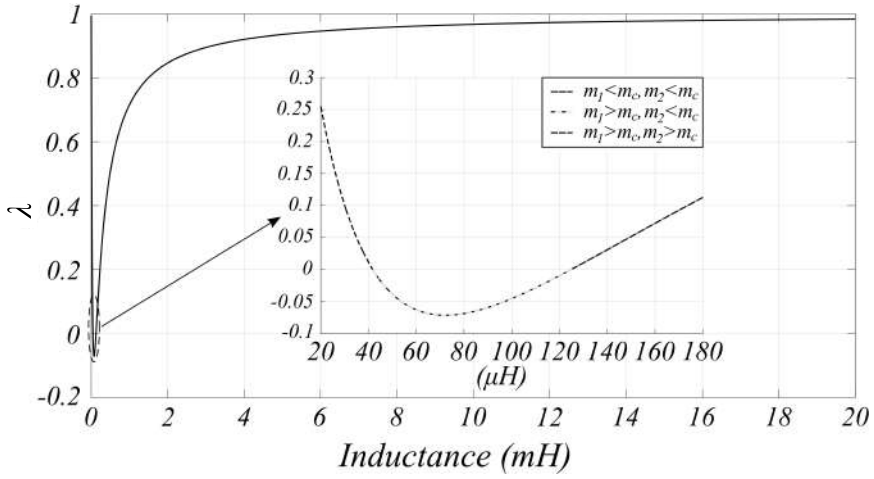


Figure 4.7: Behavior of λ with Variation of Inductance L for OCC with Triangular Carrier.

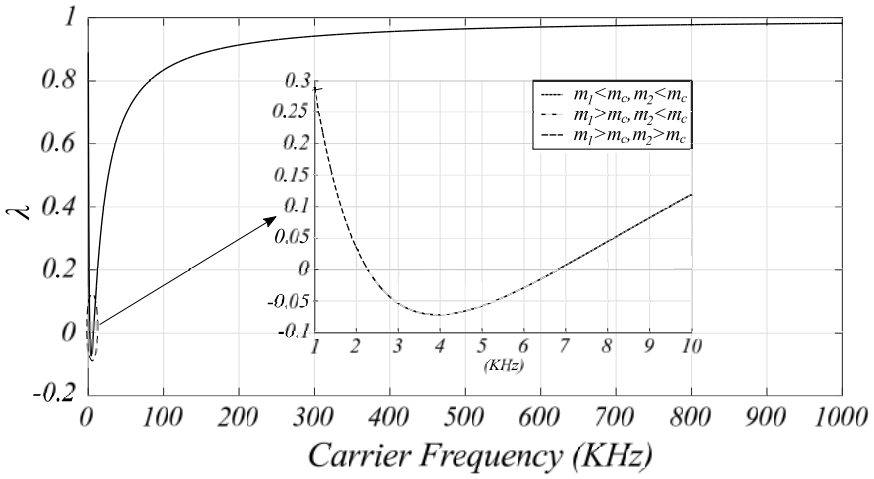


Figure 4.8: Behavior λ with Variation of Switching Frequency f_s for OCC with Triangular Carrier.

Region I In this case, the current rising slope m_1 is greater than the carrier slope m_c and the current falling slope m_1 is less than or equal to the carrier slope m_c. The convergence of the duty cycle d_n must occur in one cycle (for $\lambda = 0$) or more periods ($\lambda > 0$).

In Figure 4.9 It can be observed simulation results for the converter operating at a operation point with $\lambda = 0.5$ ($fs = 26.69$ kHz). The convergence of the duty-cycle occurs after five periods. The current ripple is 25%.

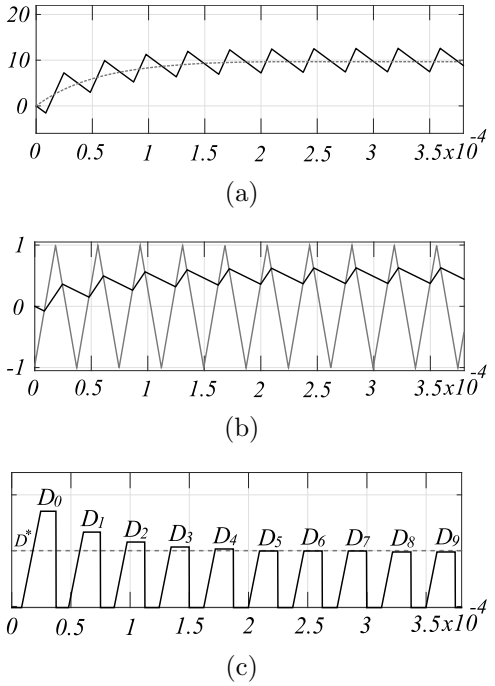


Figure 4.9: Converter response for $\lambda = 0.5$: Input current (black) and reference current from equivalent RL circuit (grey). (b) Behavior of duty-cycle over time. (c) Carrier (grey), current (black).

In Figure 4.10 It is shown the results for the converter operating with $\lambda = 0$ (f_s = 6.82 kHz). In this case the current rising slope is equal to the carrier signal slope. The convergence takes place after one cycle, as expected. However, the current ripple becomes 100%, demanding an output passive filter, which would delay the convergence time. Hence, It is a tradeoff between the response time and current ripple.

Region II In this region, $-1 < \lambda < 0$ with $m_1 > m_c$ and $m_2 < m_c$, i.e., when the instantaneous value of the current is smaller than the instantaneous value of the carrier, the PWM command inverts the switches' states so that switches q_2 e q_3 are conducing, making the current grow, however since the current slope is greater than the carrier's one, the current is soon greater than the carrier, restarting the process during the rising time interval of signal v_c. This situation is depicted in Figure 4.11.

The DC bus voltage controller will adjust its output such that the average input current is equal to that of the associated RL circuit.

Even though there is controllability in Region II, this region should be avoided, once during the rising interval of the carrier, the rising slope of the current is larger than the slope of the carrier, so that the switching frequency would be limited only by the speed response of PWM circuitry.

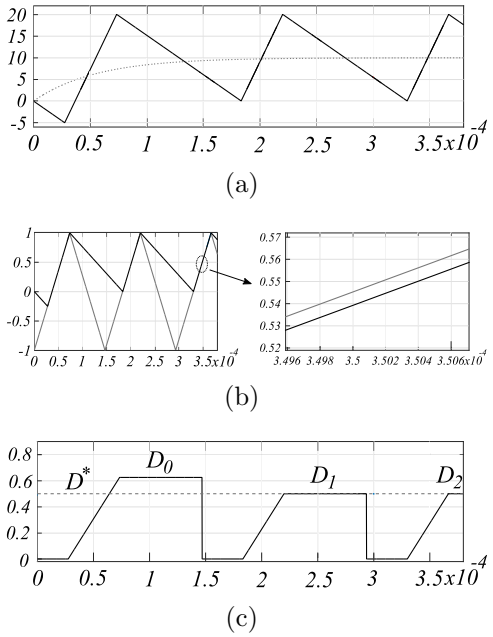


Figure 4.10: Converter Response for $\lambda = 0$. (a) Input Current (Solid) and Reference Current from Equivalent RL Circuit (Dashed), (b) Carrier (Grey), Current (black), (c) Behavior of Duty-Cycle Over Time.

Region III This region indicates the ineffectiveness of the DC bus controller, in which case the modulating signal accompanies the carrier, which translates into a triangular current with zero average.

4.2.2.1 Mandatory Minimum Inductance

Therefore, the stability condition for the OCC with triangular carrier is

$$m_c \geq m_1, \tag{4.27}$$

$$f_s \geq \frac{m+1}{4L} R_e. \tag{4.28}$$

The mandatory minimum inductance is defined as

$$L > \frac{m+1}{4f_s} \frac{V_g}{I_{gmin}} = L_{minTRI}. \tag{4.29}$$

Since $0 < m < 1$, comparing (4.1) and (4.29) it can be concluded that minimum inductance for a converter controlled by OCC with triangular carrier has lower value compared to the same converter controlled by OCC with sawtooth carrier

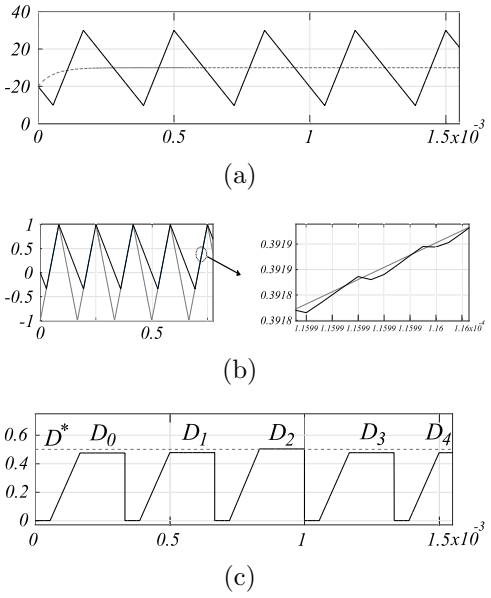


Figure 4.11: Converter Response for $\lambda < 0$. (a) Input Current (Solid) and Reference Current from Equivalent RL Circuit (Dashed), (b) Carrier (Grey), Current (Black), (c) Behavior of Duty-Cycle Over Time.

4.3 General Approach for Use of Grid Voltage Measurements in OCC

Even though OCC strategies claim for lower complexity and less use of sensors, in some application grid voltage is sensed as in GCI [31] and the so-called Fast Response One-Cycle Control (FOCC) [32]. On one hand, voltage measurements are mandatory for classical OCC strategies in GCI and for no-load operation of converters. On the other hand, the grid voltage sensed signals are used to improve dynamic response of current control. However, the use of grid voltage measurements are presented in a stratified way in Technical Literature.

In this section, a general approach for use of sensed grid voltage signals is proposed, where the grid voltage measurement gain k is associated with the minimum - or maximum - current as well as it is related with the dynamic response speed of current control.

Rewriting (3.13)

$$\bar{I}_g = \frac{1}{R_e}\bar{V}_g. \tag{4.30}$$

In [110] the therm $1/R_e$ was rewritten as function of two introduced variables K_2 and K_3

$$\frac{1}{R_e} = K_2 + K_3, \tag{4.31}$$

where K_2 is a introduced constant for limiting the maximum current and K_3 is a parameter used for controling the converter power flow.

Replacing (4.31) into (4.30) yields

$$\bar{I_g} = K_2\bar{V_g} + K_3\bar{V_g}. \tag{4.32}$$

Replacing (3.26) in (4.32) with $K_1 = 0.5$ and considering the measurement resistance R_s it leads to

$$R_s i_g = R_s K_2 v_g + R_s V_0 K_3(1 - 2d). \tag{4.33}$$

Defining

$$\begin{cases} k = R_s K_2; \\ V_{ms} = R_s V_0 K_3. \end{cases} \tag{4.34}$$

Therefore (4.34) becomes

$$R_s i_g - k v_g = V_{ms}(1 - 2d), \tag{4.35}$$

and

$$\frac{1}{V_{ms}}(R_s i_g - k v_g) = (1 - 2d). \tag{4.36}$$

These are the implementation equations for the OCC with voltage grid sensing in its Analog and Digital versions, respectively, and they are summarized in Figure 4.12. The parameter k is associated with the minimum - or maximum - current and it is related with the dynamic response speed, as it will be shown later in this section.

Replacing (4.30) into (4.35) and (4.31) into (4.34) results in

$$i_g = \frac{1}{R_s}\left(k + \frac{V_{ms}}{V_0}\right)v_g, \tag{4.37}$$

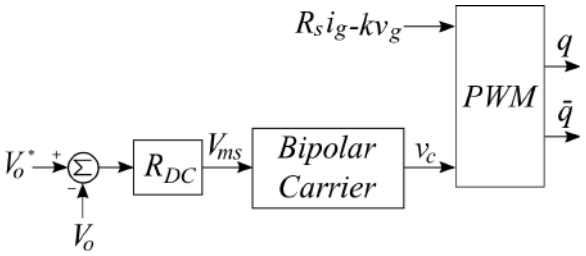
with

$$V_{ms} = V_0\left(\frac{R_s}{R_e} - k\right). \tag{4.38}$$

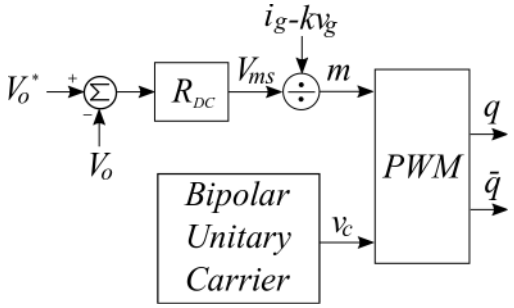
Equations above show that the average currents of the inductors are proportional to phase voltages and to V_{ms}. Note that although there is the addition of the parameter k in this relation, the signal V_{ms} embeds the subtraction of the value of k in itself, so the term K does not change the system power flow.

From (4.30) the signal V_{ms} may be defined in the form

$$V_{ms} = \frac{R_s V_o}{R_{es}}, \tag{4.39}$$



(a)



(b)

Figure 4.12: Block Diagram of OCC with Grid Voltage Measurement: (a) Analog Implementation (b) Digital Implementation.

with

$$R_{es} = \frac{R_s R_e}{R_s - K R_e} = \frac{R_e}{1 - K_2 R_e}. \tag{4.40}$$

The pole voltage v_{p1} is then given by

$$v_{p1} = mV_o = \left((R_s i_g - k v_g)\frac{R_{es}}{R_s V_o}\right)V_o = R_{es} i_g - k\frac{R_{es}}{R_s} v_g. \tag{4.41}$$

From (4.42) and (4.39) it is possible to obtain

$$\mathbf{V_g}\left(\frac{R_s}{R_s - kR_e}\right) = \mathbf{I_g} R_{es} + j\omega L \mathbf{I_g}. \tag{4.42}$$

Therefore, a new RL equivalent circuit can be derived, composed by a modified input voltage source V_g', an inductance L and a modified equivalent resistance R_{es}, in which

$$v_g' = \left(\frac{R_s}{R_s - kR_e}\right) v_g. \tag{4.43}$$

The angle displacement can be calculated by

$$\delta' = \tan^{-1}\left(\frac{\omega L_g}{R_s}\left(\frac{R_s}{R_e} - k\right)\right). \tag{4.44}$$

Therefore the PF can be regulated by k: $k > 0$ increases the PF and $k < 0$ decreases it. The theoretical limit is given by

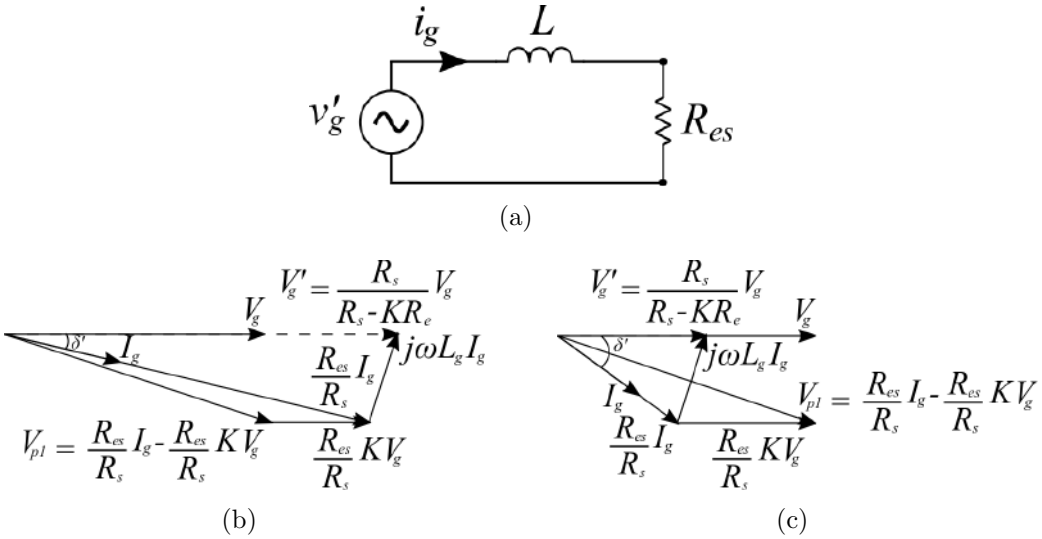


Figure 4.13: (a) Modified RL equivalent circuit; Phasor Diagram FOCC with (b) $k > 0$; (c) $k < 0$.

$$k = \frac{R_s}{R_e}. \tag{4.45}$$

This value of k is not feasible since from (4.39) $k = R_s/R_e$ would mean infinite resistance R_{es} and leading to null current.

The duty-cycle convergence D_{xn} is now based on R_{es}, which can be modified with k and a new system time constant is given by

$$\tau_1 = \frac{L}{R_{es}} = \frac{L}{R_e} \frac{(R_s - kR_e)}{R_s}. \tag{4.46}$$

Comparing with (3.62) the following relationship is obtained

$$\tau_1 = \tau_0 \frac{(R_s - kR_e)}{R_s}. \tag{4.47}$$

Therefore, the time constant is regulated by k, which has a close relationship with R_e where it has to agree with

$$R_s - kR_e > 0, \tag{4.48}$$

leading to

$$k < \frac{R_s}{R_e}. \tag{4.49}$$

The step responses for input current of a DC-DC converter controlled by OCC with $k = 0$ (conventional OCC), $k > 0$ (faster response) and $k < 0$ (slower response) are shown in Figure 4.14, corroborating with (4.47).

The gain k can assume positive or negative values and the emulated resistance

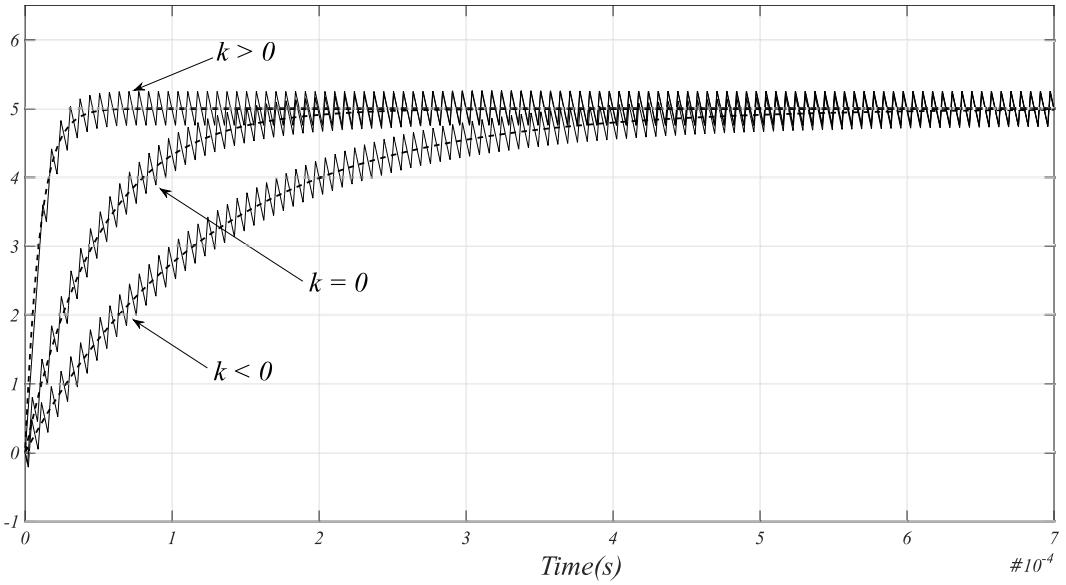


Figure 4.14: Step Responses for Input Current of a DC-DC Converter Controlled by OCC with $k = 0$ (Conventional OCC), $k > 0$ (Faster Response) and $k < 0$ (Slower Response) (1 A/div.).

$R_e > 0$ represents the operation of the converter as PFC or APF; $R_e < 0$ represents GCI operation of the converter. The operation ranges are shown in Figure 4.15.

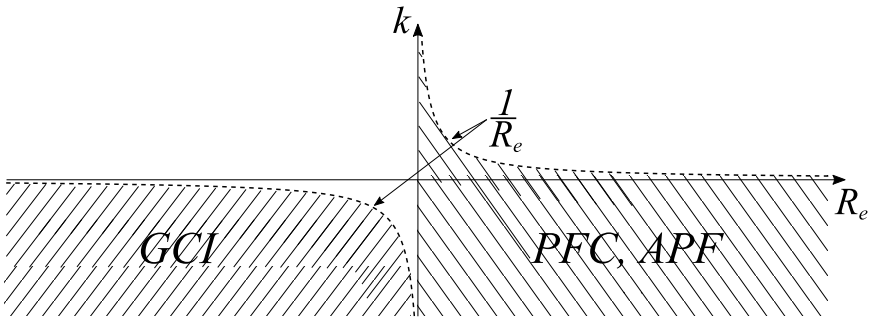


Figure 4.15: Operation Ranges of k and R_e in APF, PFC and GCI Operating Modes.

Another issue to be concerned about this technique is the stability of the system. From (4.29) the minimum inductance L for the convergence of duty cycle with the sawtooth carrier is now given by

$$L > \frac{m+1}{4f_s} R_{es} = \frac{m+1}{4f_s} \frac{R_s R_e}{R_s - kR_e}. \tag{4.50}$$

For $k > 0$ the minimum L increases, and for $k < 0$ the minimum inductance decreases. Therefore the gain k has also influence on stability of current control.

In its turn, for a given inductance L and switching frequency f_s, the maximum k can be derived from (4.50)

$$k < \frac{R_s}{R_e} - R_s \frac{m+1}{4f_s L}. \tag{4.51}$$

Comparing (4.49) and (4.51) it can be concluded that the maximum k is given by (4.51).

4.3.0.1 APF and PFC

The converter operation as APF and PFC indicates the power flow from the grid to the converter, and it is represented by $R_e > 0$. From (4.49)

$$R_e < \frac{R_s}{k}. \tag{4.52}$$

For $k > 0$ the (4.52) defines the minimum load I_{gmin} (R_{emax})

$$R_e < R_{emax} = \frac{R_s}{k}, \tag{4.53}$$

$$\Rightarrow I_g > I_{gmin} = \frac{V_g}{R_{emax}} = \frac{|k|}{R_s} V_g. \tag{4.54}$$

The time constant for this case is

$$\tau_{11} = \tau_0 \frac{(R_s - kR_e)}{R_s}. \tag{4.55}$$

The time constant τ_{11} is smaller than τ_0, leading to a wider bandwidth and a faster system response.

For $k < 0$ from (4.52) it can be concluded the system operates for any value of $|k|$.

The new time constant is

$$\tau_{12} = \tau_0 \frac{(R_s + |k|R_e)}{R_s}. \tag{4.56}$$

Therefore the time constant τ_{12} is bigger than τ_0, conducing to a narrower bandwidth and a slower system response.

The operation at null load operating point is described by the limit $R_e \to \infty$ in (4.40), leading to

$$R_{es} = \begin{cases} \frac{R_s}{k}, k < 0; \\ -\frac{R_s}{k}, k > 0. \end{cases} \tag{4.57}$$

Therefore, null load operation is possible only for $k < 0$.

4.3.0.2 GCI

For the GCI operation mode, the OCC operates with $R_e < 0$. Similarly it can be written

$$|R_e| < -\frac{1}{k}. \tag{4.58}$$

For $k < 0$ the (4.58) defines the maximum load $|I_{gmax}|$ ($|R_{emin}|$)

$$|R_e| > |R_{emin}| = \frac{1}{|k|}, \tag{4.59}$$

$$I_g < I_{gmax} = \frac{V_g}{|R_{emin}|} = |k|V_g. \tag{4.60}$$

The time constant for this case is

$$\tau_{13} = \tau_0(1 - |k||R_e|). \tag{4.61}$$

The time constant τ_{13} is smaller than τ_0, conducing to a wider bandwidth and a faster system response. Increasing $|k|$, on the other hand, decreases the maximum current.

The operation for $k > 0$ from (4.58) is prohibitive because $|R_e| > 0$.

Besides, the operation at null load operating point is described by the limit $R_e \to -\infty$ in (4.40), leading to

$$R_{es} = \frac{1}{k}, k < 0. \tag{4.62}$$

4.3.1 Three-Phase DOCC

The OCC with grid voltage measurement can also be applied APF, since increasing the current control bandwidth is a fundamental concern in current filtering.

The control law of such scheme is similar to that applied in PFC and it is given by

$$R_s \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} - k \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} = V_{ms} \begin{bmatrix} 1 - 2d_{an} \\ 1 - 2d_{bn} \\ 1 - 2d_{cn} \end{bmatrix}. \tag{4.63}$$

As seen earlier in this text, the choice of $k > 0$ enlarges the current control bandwidth, bringing improvements on harmonics correction and dynamic response, and increases the PF, however it does not allow operation with no load. On the other hand, making $k < 0$ enables the null load operation, but narrows the current controller bandwidth and decreases PF.

The OCC with grid voltage measurement technique analyzed in Subsection 4.3 is now developed for a three-phase application. The idea is the same: take measures of phase grid voltages with a gain K and sum up with the measured phase current.

This control approach is depicted in Figure 4.16.

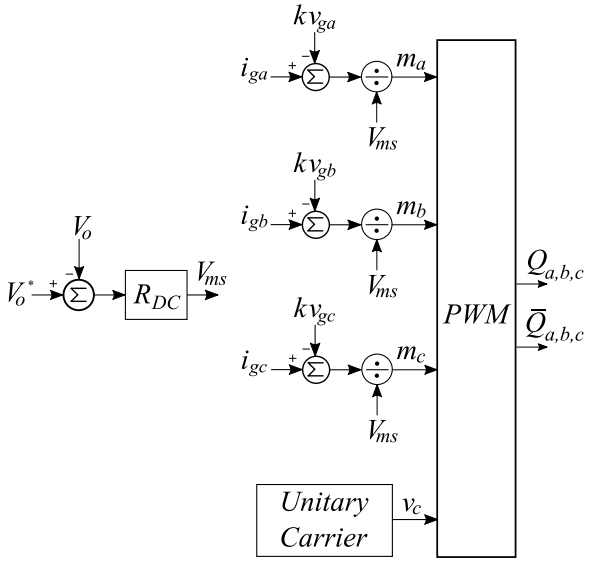


Figure 4.16: Schematic of Implementation of DOCC with Grid Voltage Measurement.

The control law of such scheme is given by

$$R_s \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} - k \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} = V_{ms} \begin{bmatrix} 1 - 2d_{an} \\ 1 - 2d_{bn} \\ 1 - 2d_{cn} \end{bmatrix}. \tag{4.64}$$

fv

The carrier amplitude V_{ms} is defined in the form

$$V_{ms} = \frac{R_s V_0}{R_{es}}, \tag{4.65}$$

with

$$R_{es} = \frac{R_s R_e}{R_s - K R_e} = \frac{R_e}{1 - k_2 R_e}. \tag{4.66}$$

Similarly to the single-phase case, the three-phase system time constant is defined as

$$\tau_1 = \frac{L}{R_{es}} = \frac{L}{R_e}(1 - k_2 R_e), \tag{4.67}$$

thus

$$\tau_1 = \tau_0(1 - k_2 R_e). \tag{4.68}$$

Consequently, the time constant is regulated by K, which has a close relationship with R_e, where it has to agree with

$$1 - k_2 R_e > 0, \tag{4.69}$$

leading to

$$k_2 < \frac{1}{R_e}. \tag{4.70}$$

As seen in Subsection 4.3, the operation with $k > 0$ leads to a system with faster dynamic response with prohibitive operation at null load operating point. On the other hand, application of $K < 0$ conduces to slower dynamics and allows null load operation.

4.4 Frequency Analysis of Analog OCC

Considering the Single-phase Full-Bridge Rectifier controlled by OCC depicted in Figure 4.17, the averaged model is obtained through a small signal analysis in B and can be summarized in

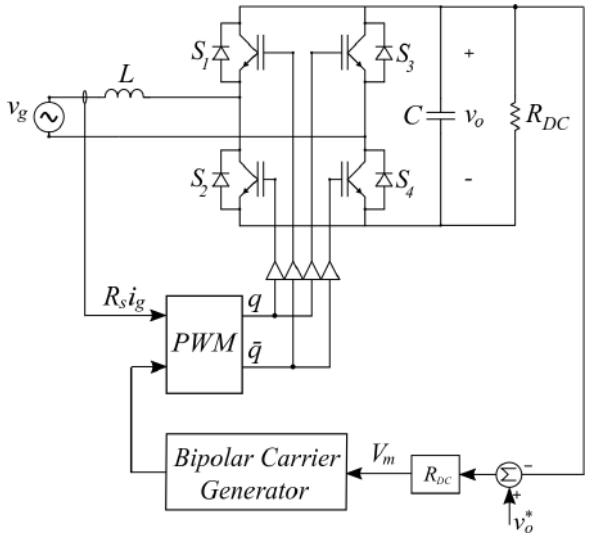


Figure 4.17: Model of Single-phase Full-Bridge with OCC.

$$H_1(s) = \frac{\hat{V}_o(s)}{\hat{D}(s)} = 2\frac{\bar{v_g}(t)}{(1-2\bar{D})^2} \frac{1 - s\frac{L}{(1-2\bar{D})^2 R_{DC}}}{\frac{LC}{(1-2\bar{D})^2}s^2 + \frac{L}{(1-2\bar{D})^2 R_{DC}}s + 1}, \tag{4.71}$$

$$H_2(s) = \frac{\hat{I}_g(s)}{\hat{D}(s)} = 2C\frac{\bar{v_g}(t)}{(1-2\bar{D})^3} \frac{s + \frac{2}{R_{DC}C}}{\frac{LC}{(1-2\bar{D})^2}s^2 + \frac{L}{(1-2\bar{D})^2 R_{DC}}s + 1}, \tag{4.72}$$

where H_1 and H_2 are the duty-cycle to line current and Bus voltage Transfer Functions, respectively.

The small signal model of the control scheme of Figure 4.17 is depicted in Figure 4.18, where there is an inner loop T_i called current loop which has a faster dynamic

response compared to the external loop T_v, the voltage loop [111].

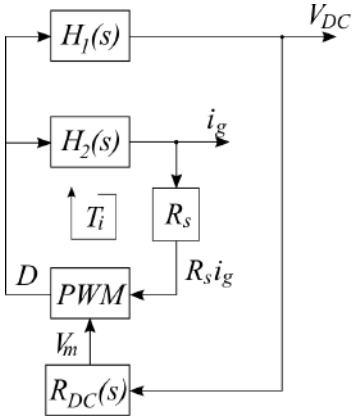


Figure 4.18: Small Signal Block Diagram of OCC.

The current loop gain is given by

$$T_i = H_2(s) R_s F_m(s), \tag{4.73}$$

where H_2 is the duty-cycle-to-inductor-current transfer function given by (4.72), R_s is grid current sensor output resistance and F_m is the small-signal gain of the bipolar analog PWM modulator and is given in [112] by

$$F_m(s) = \frac{\hat{D}(s)}{\hat{V_{ref}}(s)} = \frac{1}{2V_m}. \tag{4.74}$$

The current loop gain is then given by

$$T_i = 2C \frac{\bar{v_g}(t)}{(1-2\bar{D})^3} \frac{s + \frac{2}{R_{DC}C}}{\frac{LC}{(1-2\bar{D})^2}s^2 + \frac{L}{(1-2\bar{D})^2 R_{DC}}s + 1} R_s \frac{1}{2V_m}. \tag{4.75}$$

The current loop gain varies with the line voltage V_g, the load R_{DC} and with parameters of the converter inductance L and capacitance C. The analysis of the effect of variations on these parameters is presented below.

First, the analysis is done with the converter of Figure 4.17 in a operating point with the parameters defined in Table 4.4

For this parametrization, the current loop gain is obtained and is shown in Figure 4.19

Observe that the current loop has its cross-over frequency equal to the corner frequency of the RL equivalent circuit with $L = 1mH$ and $R = R_e = 20\Omega$. The dynamic response of the current control is therefore equivalent to the dynamics of a RL circuit with resistance R_e, which corroborates with the strategy to control the converter to emulate a resistor studied in 3.2.

Following, the effect of variation of the rectifier load is analyzed. In Figure 4.20 are depicted the Bode plots of the current gain for different load values. Increasing

Table 4.1: Operating Point Parameters of a current loop gain for Single-phase Full-Bridge OCC controlled converter

Parameter	Value
v_g	$100.0V$
V_0	$200.0V$
C	$1.0mF$
L	$1.0mH$
R_{DC}	80.0Ω
f_s	$150.0kHz$

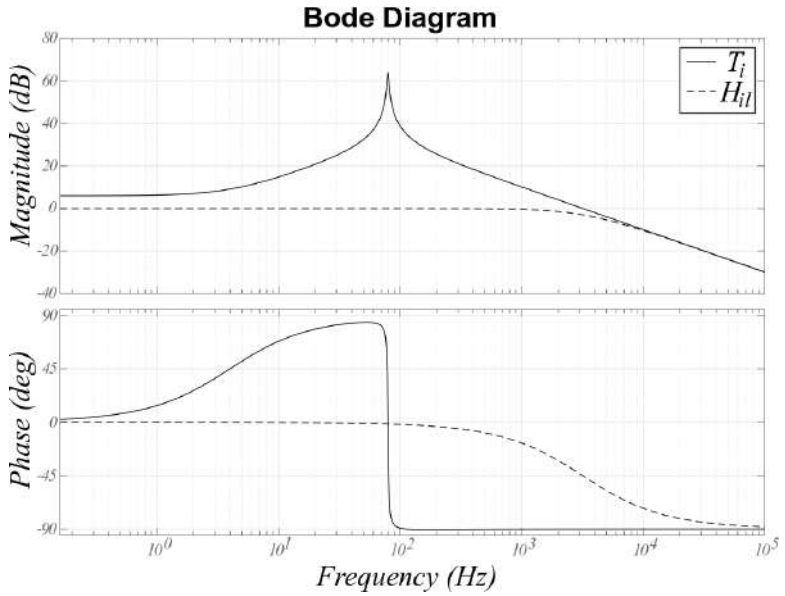


Figure 4.19: Bode plot - Current Loop Gain for Full-Bridge Boost Converter with Load and for RL circuit response.

R_{DC} (decreasing Output Power) enlarges the cross-over frequency of the current loop gain.

On the other hand, the bode plots for variation of input voltage are shown in Figure 4.21. It can be seen that the crossover frequency does not depend on the line voltage V_g.

The bode plots for the variation of DC bus capacitance C show that changes in C do not influence the cut-off frequency, i.e., the time response of the current control.

The influence of variation of converter inductance L on the dynamic response of the system is depicted in Figure 4.23. Increasing the inductance L decreases the system time constant τ, and vice-versa.

The input current ripple of the converter of Figure 4.17 can be calculated from examination of Figure 4.24. Reminding that in an inductor $v_L(t) = Ld/dti_L(t)$, and taking the input current rising slope into consideration leads to

$$\Delta I_L = \frac{1}{L}\int_0^{DT_s} v_L(t)dt = \frac{1}{L}\int_0^{DT_s} (V_o + v_g)dt. \tag{4.76}$$

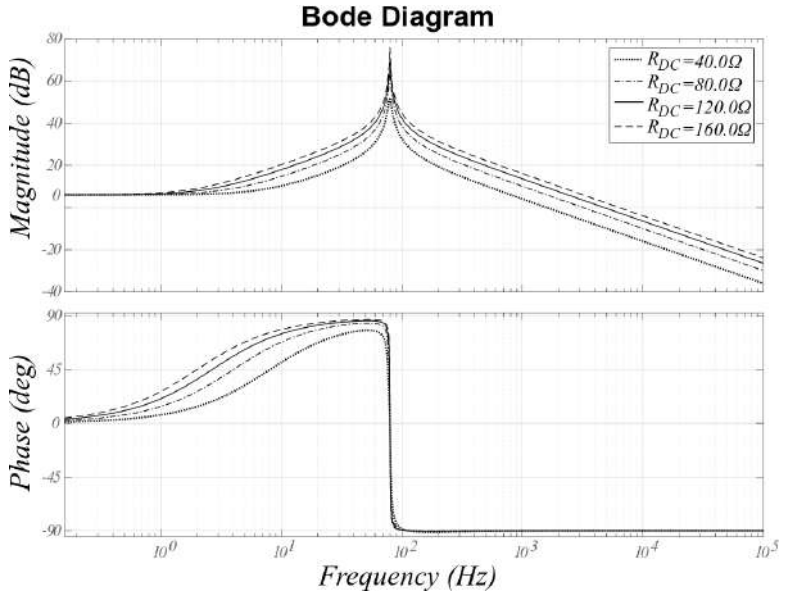


Figure 4.20: Bode Plot - Variation of Current Loop Gain for Full-Bridge Boost Converter with Load Variation.

Resolving and considering (3.28) brings

$$\Delta I_L = \frac{(V_o^2 - v_g^2)}{2V_o f_s L}. \tag{4.77}$$

A smaller inductance leads to a bigger current ripple. Therefore a trade-off between current ripple and system response must be taken into account on system and control designs. The variation of f_s does not change the system response [32] but the current ripple.

In Figure 4.25 is depicted the frequency response for the system with change of gain k. The system response with $k = 0$ has intermediate cut-off frequency. For $k > 0$ the cut-off frequency increases, and for $k < 0$ the cut-off frequency decreases. This behavior corroborates with (4.46), with faster response for $k > 0$ and vice-versa.

4.5 Frequency Analysis Digital OCC

Compared to analog control the main characteristic that distinguishes the digital control loop is the presence of some delays which can affect frequency response and therefore should be taken into account in modeling and control designing processes.

In this work the delay time for A/D conversion followed by the execution time of the control algorithm by the CPU called *Control Delay* is neglected. Hence, only the effect of the modulation delay will be considered.

The two main approaches for digital control design are:

1. based on the discrete-time modeling approach, with no averaging paradigm in the process of modeling;

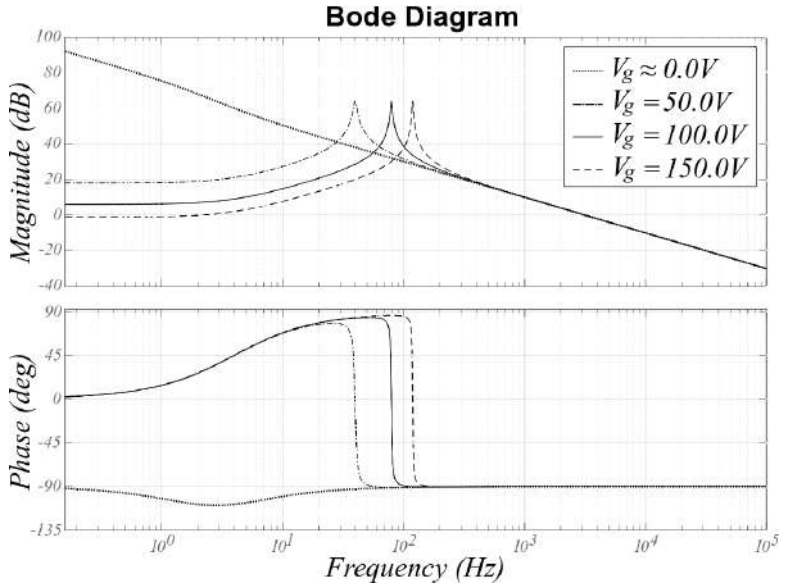


Figure 4.21: Bode plot - Variation of Current Loop Gain for Full-Bridge Boost Converter with Input Voltage.

2. embedding the time delay into the averaged small-signal model [112].

For the second approach, however, it is important to have in mind that including the delay effects into the averaged modeling is possible but only in an approximate manner. In fact, since the averaging approach neglects the converter high-frequency dynamics, the inherent aliasing effects owned to sampling operation, which can affect the low-frequency range as well, are not accounted for. Therefore, this approach can be used only when it can be assumed that the sensed signal is sampled at approximately at its average value, so that aliasing effects can be neglected.

The two main scenarios of small-aliasing are highlighted:

- the sensed signal is an well-filtered signal such as the output voltage, which has mainly the DC-component, then the sensed signal will be approximately the average signal;

- the signal is sensed at an instant when the ripple component is approximately zero, as in sampling the inductor current at valley point instant of symmetrical modulation as depicted in Figure 4.26.

The sampling of inductor current at valley and peak point instants are specially interesting for OCC strategies, since they result in sensing of average inductor current. Therefore no averaging methods are demanded with DOCC for this sampling strategy.

The uniformly-sampled Pulse-Width Modulator usually available in modern micro-controllers, disregarding quantization effects, can be modeled as an analog

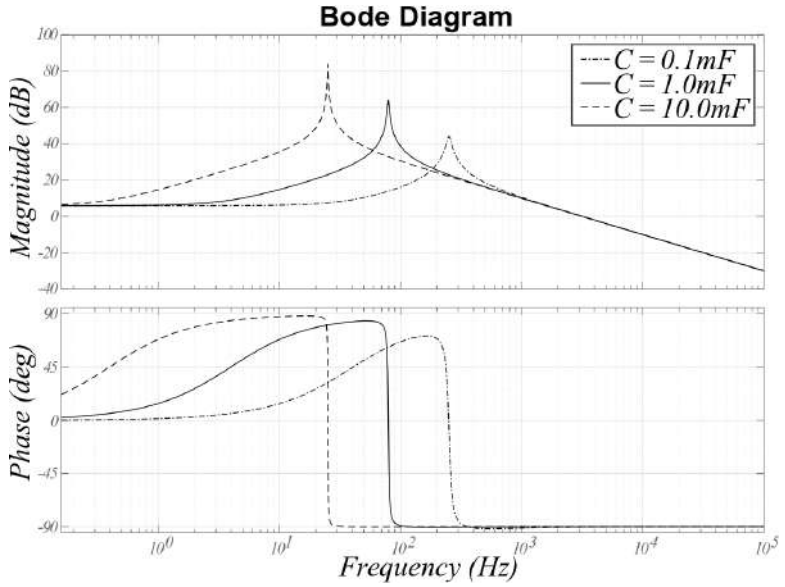


Figure 4.22: Bode plot - Variation of Current Loop Gain for Full-Bridge Boost Converter with Input DC-Bus Capacitance Variation.

Table 4.2: Laplace-Domain models for Uniformly-Sampled Pulse-Width Modulators

PWM modulator	$H_e(s)$
Trailing-edge	e^{-sDT_s}
Leading-edge	$e^{-s(1-D)T_s}$
Symmetrical	$\frac{1}{2}(e^{-s\frac{(1-D)T_s}{2}} + e^{-s\frac{(1+D)T_s}{2}})$

PWM comparator, a Zero-Order-Holder (ZOH) on its input and a sampler as illustrated in Figure 4.27. The input $u(t)$ is sampled synchronously at the beginning of the PWM cycle and sent to the ZOH. Then, the value at the output of the ZOH is compared with the carrier.

Depending on the type of the carrier different types of uniformly-sampled pulse-width modulators can be obtained. The table 4.5 is derived in [113] and summarizes the models for uniformly-sampled PWM for different carrier waveforms, with waveforms summarized in Figure 4.28

Based on *small-aliasing approximation* condition, only the Symmetrical Triangular Carrier will be considered for modeling purposes in this work.

The small signal diagram block is shown in Figure 4.29. The measured current passes through the modulation delay block $H_e(s)$ and its result is divided by the output of the DC-bus controller, and then through the PWM block to generate the duty cycle signal.

The Current Loop Gain for digital OCC controlled full-bridge boost converter in shown in Figure 4.30. In this case, the response is practically the same as the analog case. But close to the Nyquist frequency the frequency response diverges.

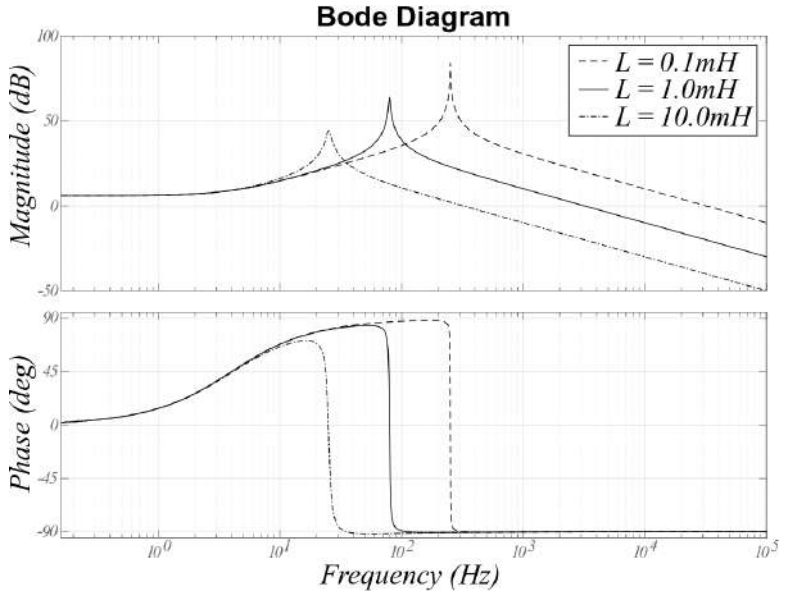


Figure 4.23: Bode plot - Variation of Current Loop Gain for Full-Bridge Boost Converter with Inductance Variation.

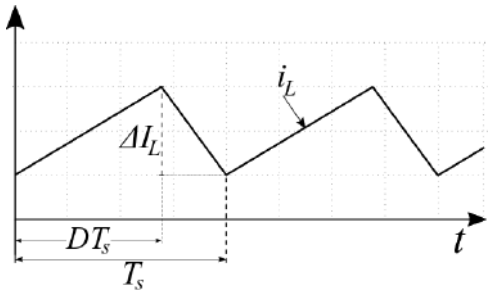


Figure 4.24: Instantaneous Inductor Current with Constant Input and Output Voltage.

4.6 Improvements on Feedforward Inductive Voltage Drop Compensation

The strategy used to compensate the inherent inductive voltage drop of OCC technique seen in Section 3.6 is based on estimation of inductive voltage drop based on system parameters and on the estimation of the quadrature current by two second order LPF, which results in a 4th order transfer function.

It is well known in Literature the adaptive filter Second Order Generalized Integrator (SOGI) which works as second order band-pass filter and signal orthogonalizer and has simple implementation [114]. The SOGI structure consists of two closed-loops, with the inner loop with two integrators and tuned at cut-off frequency ω', while in the outer loop is the damping factor k which determines the bandwidth and therefore the filtering capability and dynamical response as shown in Figure 4.31.

The characteristic input-to-quadrature-output transfer function of the SOGI is given by

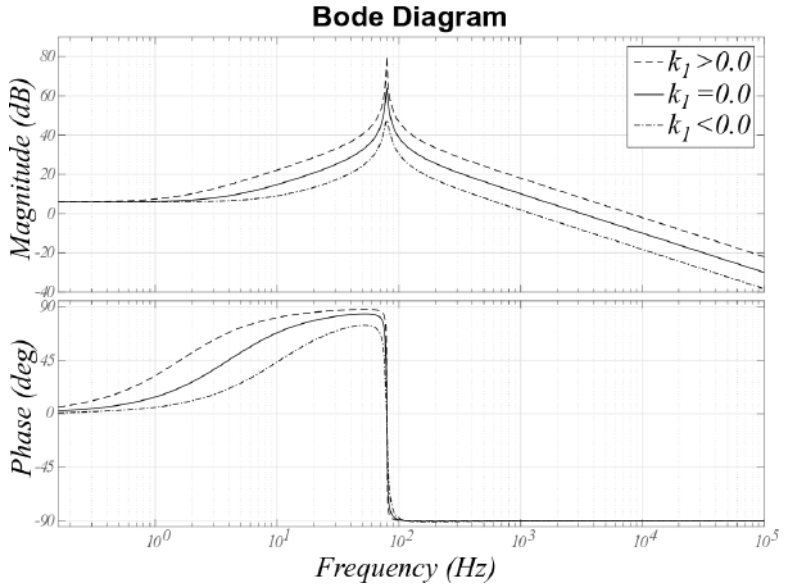


Figure 4.25: Bode plot - Variation of Current Loop Gain for Full-Bridge Boost Converter with OCC with Grid Voltage Measurement.

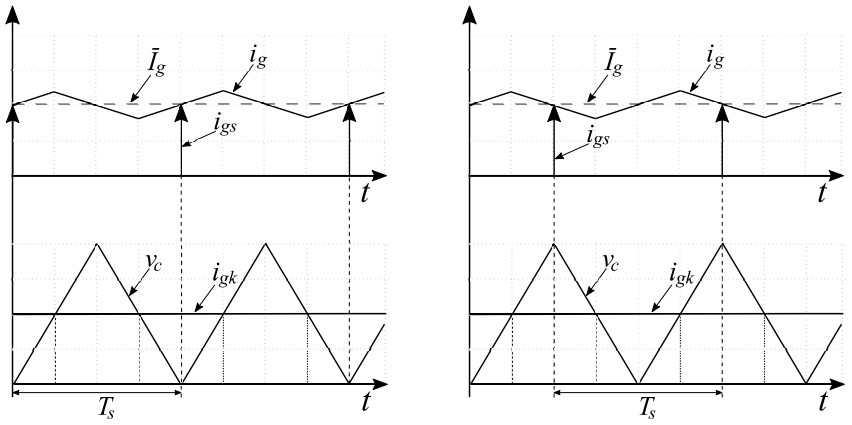


Figure 4.26: Sampling Strategy for Inductor Current of Symmetrical Modulation PWM: (a) Valley Point Instant, (a) Peak Point Instant.

$$Q(s) = \frac{V_q(s)}{V_{in}(s)} = \frac{k_f \omega'^2}{s^2 + k_f \omega' s + \omega'^2}. \tag{4.78}$$

Observe that the input-to-quadrature-output transfer function of the SOGI is 2nd order transfer function. This results in simpler implementation compared to the structure of two 2nd order LPF presented in Section 3.6.

The bode plot of the SOGI is shown in Figure 4.32 for three different values of k_f. The lower the k_f the narrower the bandwidth which brings better filtering capability but with the expense of worse dynamical response. Therefore a trade off must be taken in account when selecting the value of k_f.

From Figure 4.32 if the actual input signal frequency ω' is different from the

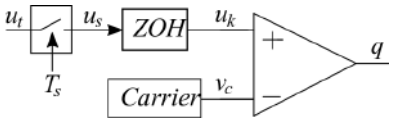
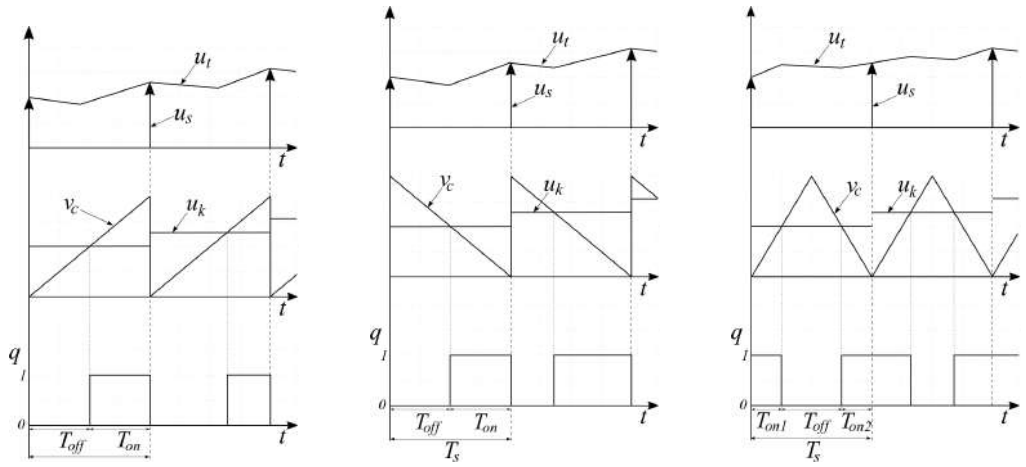


Figure 4.27: General Model for Uniformly-Sampled PWM Modulator



(a) (b) (c)

Figure 4.28: Uniformly sampled Pulse Width Modulators: (a) Trailing Edge Sawtooth Carrier, (b) Leading Edge Sawtooth Carrier (c) Symmetrical Triangular Carrier

tuned frequency ω', the signal v_q will diverge from the 90^{o} lag phase shift which is intended to be realized. The inductive drop compensation is therefore degraded.

Now, the full-bridge single phase boost rectifier studied in this chapter is simulated to show the effect of grid frequency variation on the angle displacement between grid voltage and current. The results are shown in Figure 4.33 for the converter operating with and without inductive voltage drop compensation. It can be observed that displacement angle has been reduced from the range of -16.45$^{\text{o}}$∼-20$^{\text{o}}$ to the range of -3∼3 degrees. The remaining displacement angle is due to the fixed cut-off frequency of SOGI structure. One solution is to combine the SOGI with a Frequency-Locked Loop (FLL) structure, which calculates the grid frequency.

4.7 DOCC with HPWM

The OCC with HPWM approach studied in Section 3.5 can be extended to DOCC applied to three-phase converters to take advantages of enhanced performance on output voltage synthesis and DC-bus utilization.

From (3.33) the control of three-phase DOCC is described by control law

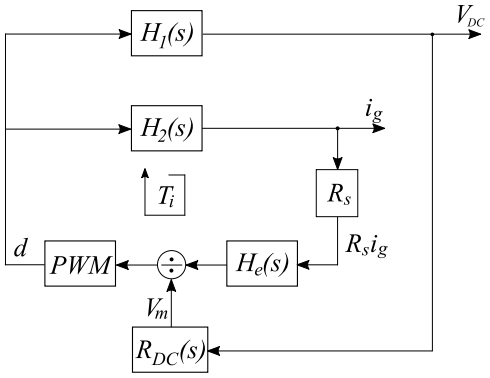


Figure 4.29: Small Signal Block Diagram - Digital OCC

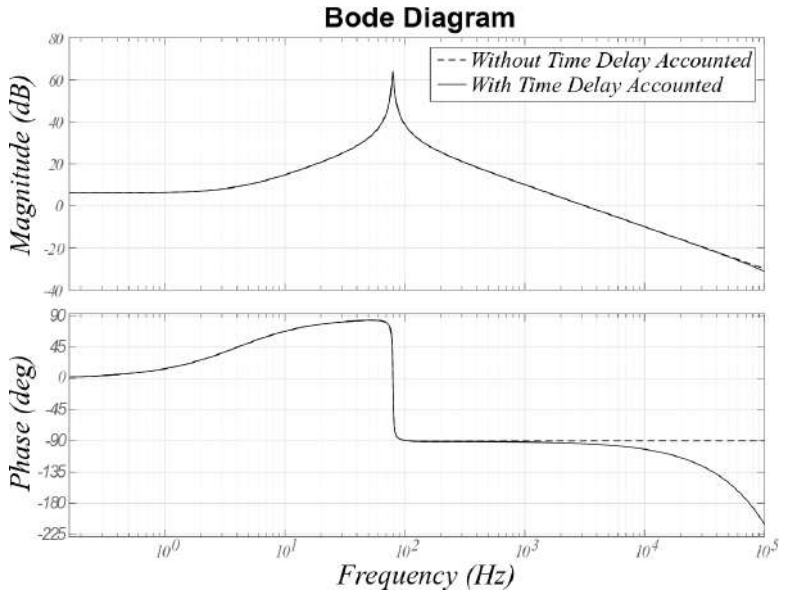


Figure 4.30: Bode plot - Influence of Time Delay Accounted to the Model.

$$\begin{bmatrix} m_a \\ m_b \\ m_c \end{bmatrix} + \begin{bmatrix} m_{N0} \\ m_{N0} \\ m_{N0} \end{bmatrix} = \begin{bmatrix} 1 - d_{an} \\ 1 - d_{bn} \\ 1 - d_{cn} \end{bmatrix}. \tag{4.79}$$

where m_x is the modulating signals for $x = a, b, c$ and m_{N0} is the common mode modulation signal given by

$$m_{N0} = \frac{1}{2} - \mu(1 + m_{min} - m_{max}). \tag{4.80}$$

The Digital OCC with HPWM is based on the injection of an appropriate zero sequence component into the modulating signals by choosing $0 \geq \mu \geq 1$, as seen earlier. The signals m_{min} and m_{max} are the minimum and maximum modulation signals among m_a, m_b, m_c.

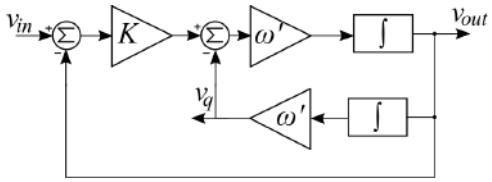


Figure 4.31: SOGI Schematic.

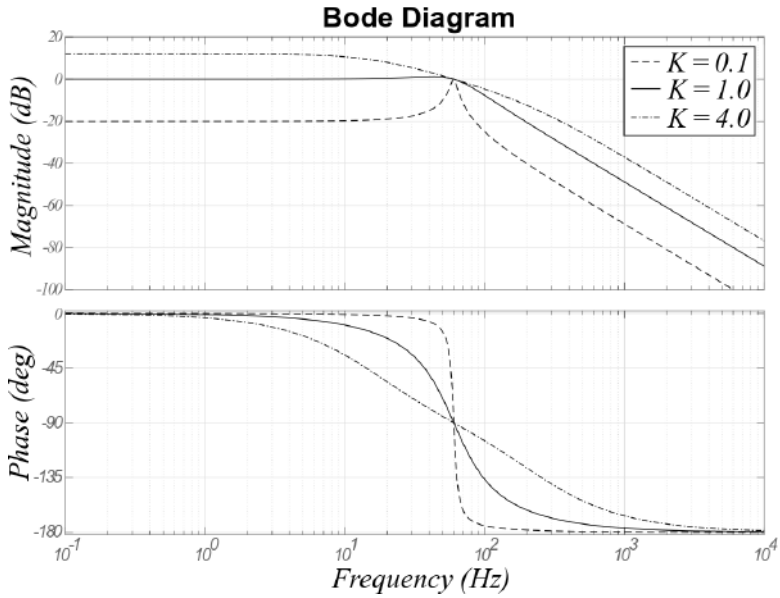


Figure 4.32: Bode Plot - SOGI Dynamics with Variation of Gain K.

4.8 Partial Conclusions

In this Chapter it has been presented some contributions for the field of One Cycle Control. First, it was studied the stability of OCC with triangular carrier through Poincaré Maps, where it was found that the use of triangular carrier enhances system stability compared to sawtooth carrier OCC.

The use of Saddle PWM OCC allows improvements on DC bus utilization by about 15.5%, and concerning loss minimization for the cases with $\lambda = 0.0$ and

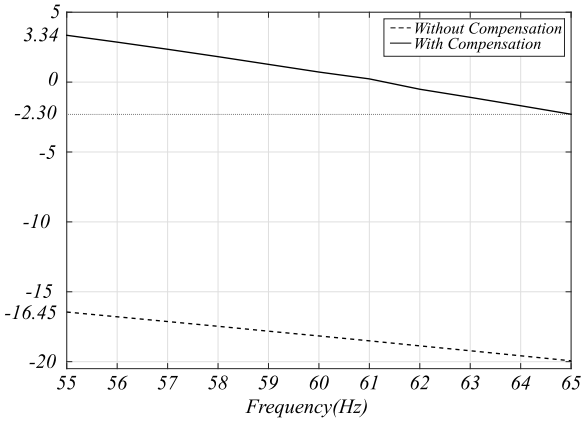


Figure 4.33: Displacement Angle with Variation of Grid Frequency.

$\lambda = 1.0$, realization of only one null vector with expected loss minimization by about 1/3.

Yet, the conventional control techniques for PFC Rectifier and APF had been presented with introduction of their general aspects and basic control design for simulation and experimental implementations.

Chapter 5

Simulation Results of Medium Power Level Model

5.1 Introduction

The three-phase PFC Rectifier and APF studied throughout this text are now tested through simulations carried out in PSIM environment for DOCC and Conventional Controllers.

The PFC Rectifier will be controlled by two different digital control techniques: DOCC and conventional dq-PWM. Likewise, the APF will be controlled by two distinct techniques: digital OCC control and pq-theory-based with dq-PWM and hystersis current control techniques. Comparative analysis of steady-state results will be carried out concerning the quantitative and qualitative metrics on PF and THD.

5.2 Three-Phase PFC

In this section, the three-phase boost PFC Rectifier is studied through simulations. The circuit schematics of the system is depicted in Figure 5.1. It consists of a grid, modeled as an ideal three-phase voltage source, and a boost converter working as a rectifier. The control and modulation block receives the grid currents and DC-bus voltage and for some strategies, also the grid voltages are received, for by means of control and modulation, defining the switches gates signals for the converter.

The parameterization of the system is done aiming to application of the control systems to industrial power level systems, with rated power of $10.0kW$.

The grid is modeled as an ideal three-phase source with nominal amplitude voltage of $V_{g_{PEAK}} = 392.0V$ ($480.0V_{ll_{RMS}}$) according to North American LV distribution network [115].

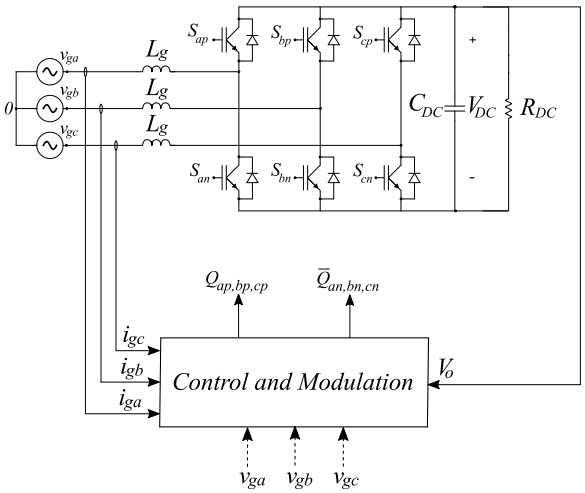


Figure 5.1: Circuit Schematics of Model of Medium Power Level Three-Phase Full-Bridge PFC Rectifier.

The inductances L_g were chosen based on (4.22) obtaining $L_g = 3.48mH$ for $\lambda \approx 0.75$ and $L_g = 12.51mH$ for $\lambda \approx 0.9$, aiming to evaluate the system response with higher and lower inductance values.

The parameters are summarized in Table 5.2.

Table 5.1: Parameters for Simulations of Medium Power Level Three-Phase Full-Bridge PFC Rectifier Model.

Parameter	Value
P	$10.0kW$
$V_{g_{PEAK}}$	392.0 V
V_{DC}	1120.0 V
C_{DC}	$1.0mF$
R_{DC}	125.0Ω
m	0.7
f_s	$30kHz$

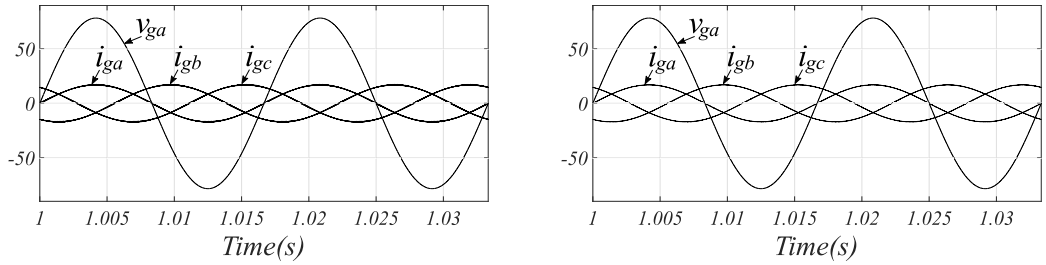
The performance of three-phase PFC Rectifier is comparatively analyzed for the system controlled by Conventional dq-PWM and for DOCC strategies.

5.2.1 Conventional dq-PWM

As presented in Chapter 2, the conventional dq-PWM control is a cascade technique with an inner control loop based on current regulation on synchronous reference frame, and an outer controlling the DC bus voltage. The main advantage is the guaranteed unit PF. The main disadvantages are the relatively complex structure and the presence of a PLL circuit which is used to provide the reference angle to direct and inverse Park Transforms.

The simulations are done then with the system controlled by Conventional dq-

PWM and the results are shown in Figure 5.2 for $L_g = 3.48mH$ and $L_g = 12.51mH$. The PF and THD of each case are shown in Table 5.2.



(a) (b)

Figure 5.2: Simulation Results for Medium Power Level Three-Phase Full-Bridge PFC Rectifier Model with Standard dq-PWM Control - Phase Voltage a (5 V/div.) and Phase Currents (1 A/div.): (a) $L_g = 3.48mH$, (b) $L_g = 12.51mH$.

Table 5.2: Simulation Results for Medium Power Level Three-Phase Full-Bridge PFC Rectifier Model with Standard dq-PWM control.

$L_g(mH)$	THD (%)	PF
3.48	1.86	> 0.99
12.51	0.522	> 0.99

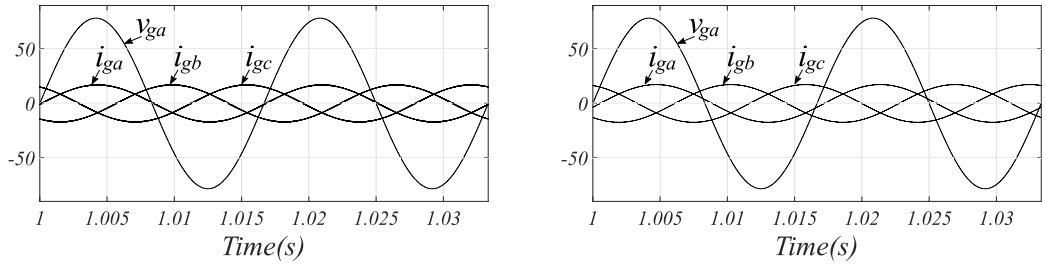
It can be seen that for the three-phase PFC Rectifier controlled by Conventional dq-PWM at steady-state the PF is almost unitary for both inductance values due to the presence of a PLL circuit in the control strategy. The THD results has shown very good performance of this control to PFC rectifier application. Further, it can be seen that the inductance has strong influence on THD results at steady state, since it filters the high-order current harmonics, reducing the current ripple.

5.2.2 DOCC

As seen in Chapters 3 and 4 DOCC strategies bring some enhancements compared to the conventional analog OCC, as seen earlier, such as modification on dynamic response with sensing of grid voltage, compensation of inductive voltage drop with a feed forward strategy, improved performance on output voltage synthesis and DC-bus utilization with DOCC with HPWM.

The results for the DOCC strategy with only current sensing for $L_g = 3.48mH$ and $L_g = 12.51mH$ are shown in Figure 5.3 and Table 5.2.2.

For both inductance values, the PF and THD has shown satisfactory results. Besides, it can be seen that the PF have influence of inductance L_g: increasing L_g decreases PF due to inductive voltage drop, as studied in Chapter 3, but because the load is light, the effects of this drop are not determinant to PF results. Concerning



(a) (b)

Figure 5.3: Simulation Results for Medium Power Level Three-Phase Full-Bridge PFC Rectifier Model with DOCC - Phase Voltage a (5 V/div.) and Phase Currents (1 A/div.): (a) $L_g = 3.48mH$, (b) $L_g = 12.51mH$.

Table 5.3: Simulation Results for Medium Power Level Three-Phase Full-Bridge PFC Rectifier Model with DOCC.

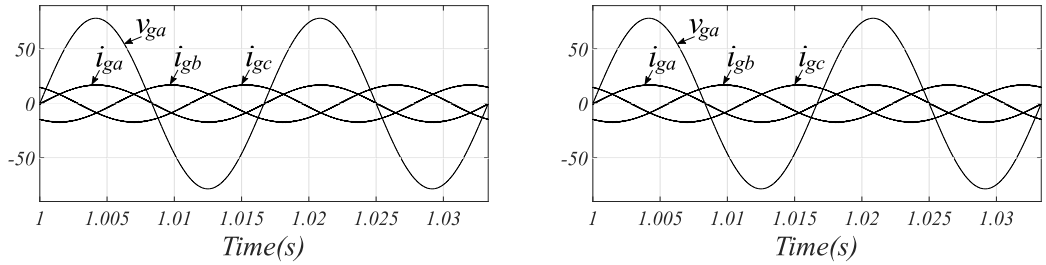
$L_g(mH)$	THD (%)	PF
3.48	1.85	> 0.99
12.51	0.5	> 0.98

THD, results have shown the inductance value has strong influence on it, similarly to the results with system controlled by Conventional dq-PWM.

5.2.2.1 DOCC with Grid Voltage Measurement

The general approach for use grid voltage measurement presented in Section 4.3 is now applied with DOCC to three-phase PFC rectifier in the simulations for different values of k and for two inductance values $Lg = 3.48mH$ and $L_g = 12.51mH$.

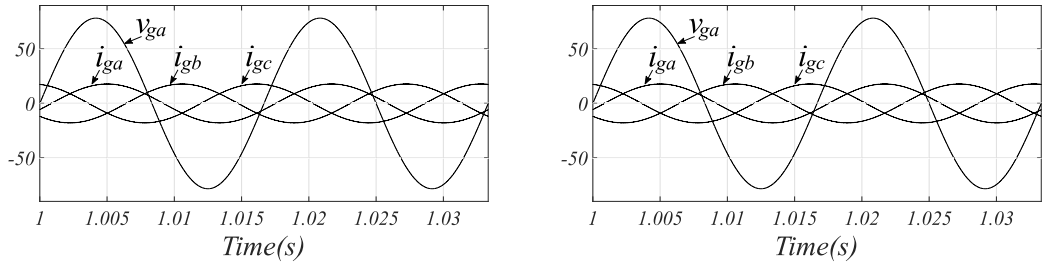
The simulation results are shown in Figures 5.4-5.5 and Table 5.4.



(a) (b)

Figure 5.4: Simulation Results for Medium Power Level Three-Phase Full-Bridge PFC Rectifier Model with DOCC With Grid Voltage Measurement for $k = 0.025$ (faster) - Phase Voltage a (5 V/div.) and Phase Currents (1 A/div.): (a) $L_g = 3.48mH$, (b) $L_g = 12.51mH$.

For the three-phase PFC Rectifier controlled by DOCC with grid voltage measurement at steady-state it can be seen that the PF have influence of gain k. However, since the load is light, the effect on PF with variation of k is not so significant,



(a) (b)

Figure 5.5: Simulation Results for Medium Power Level Three-Phase Full-Bridge PFC Rectifier Model with DOCC With Grid Voltage Measurement for $k = -0.025$ (slower) - Phase Voltage a (5 V/div.) and Phase Currents (1 A/div.): (a) $L_g = 3.48mH$, (b) $L_g = 12.51mH$.

Table 5.4: Simulation Results for Medium Power Level Three-Phase Full-Bridge PFC Rectifier Model with DOCC with Grid Voltage Measurement.

	k = -0.025		k = 0.025	
L_g	THD(%)	PF	THD(%)	PF
$3.48mH$	1.85	> 0.99	1.85	> 0.99
$12.51mH$	0.48	0.9483	0.52	> 0.99

even though these effects occur as derived in Section4.3: increasing k improves PF, and vice-versa. Concerning THD, results have shown that gain k which has low effect on it.

5.2.2.2 DOCC with Feed-forward Inductive Voltage Drop Compensation

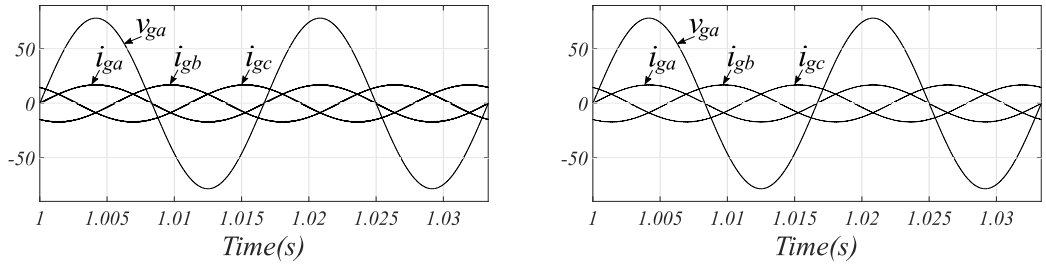
The modified feed-forward strategy for compensation of inherent inductive voltage drop proposed in Section 4.6 is applied to the simulated system. No measurements of grid voltage are taken into account.

The results are shown in Figure 5.6 and Table 5.2.2.2 for $L_g = 3.48mH$ and $L_g = 12.51mH$.

Table 5.5: Simulation Results for Medium Power Level Three-Phase Full-Bridge PFC Rectifier Model with DOCC with Inductive Voltage Drop Compensation.

$L_g(mH)$	THD (%)	PF
3.48	1.86	> 0.99
12.51	0.52	> 0.99

It can be seen from the results from Table 5.2.2.2 and 5.2.2 that the modified strategy for compensation of inductive voltage drop is effective on PF correction. Furthermore, it has no apparent influence on THD.



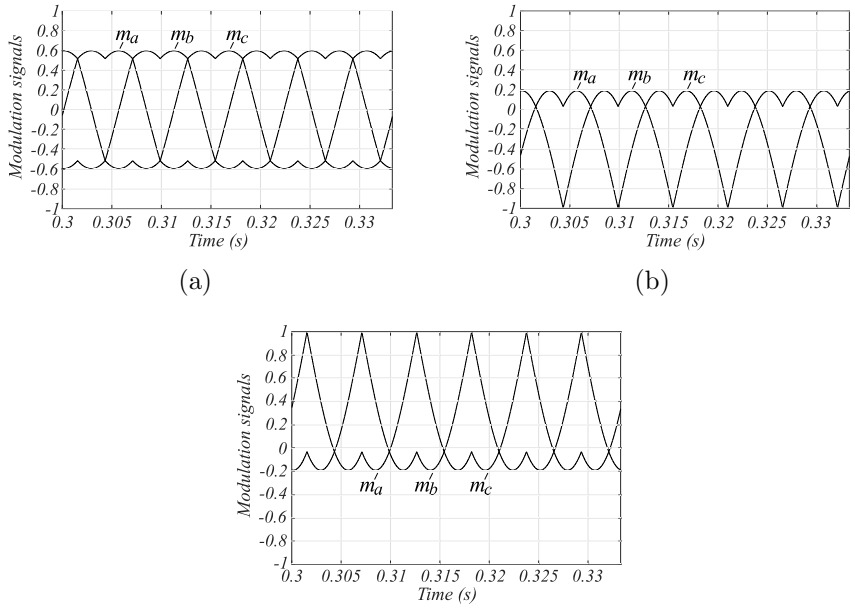
(a) (b)

Figure 5.6: Simulation Results for Medium Power Level Three-Phase Full-Bridge PFC Rectifier Model with DOCC With Feed-forward Inductive Voltage Drop Compensation - Phase voltage a (5 V/div.) and Phase Currents (1 A/div.): (a) $L_g = 3.48mH$, (b) $L_g = 12.51mH$.

5.2.2.3 DOCC with HPWM

The Hybrid PWM approach applied to DOCC which has been presented in 4.7 is now carried out in the simulated system for $\mu = 0.0$, $\mu = 0.5$ and $\mu = 1.0$. As seen earlier, $\mu = 0.0$ and $\mu = 1.0$ reduces the switching by 33% but increases the THD, while $\mu = 0.5$ conduces to better THD. The grid voltage measurements and inductive voltage drop compensation are not considered in this simulation.

The results are shown in Figure 5.7 and Table 5.6.



(a) (b)

(c)

Figure 5.7: Simulation Results for Medium Power Level Three-Phase Full-Bridge PFC Rectifier Model - Modulation Signals for DOCC with HPWM: (a) $\mu = 0.5$, (b) with $\mu = 0.0$, (c) $\mu = 1.0$.

Comparing the results from Tables 5.6 and 5.4 for $k = 0.0$, it can be observed that the variation of μ has minor influence on PF. On the other hand, the application

Table 5.6: Simulation Results for Medium Power Level Three-Phase Full-Bridge PFC Rectifier Model with DOCC with HPWM.

	$\mu = 0.0$		$\mu = 0.5$		$\mu = 1.0$	
L_g (mH)	THD(%)	PF	THD(%)	PF	THD(%)	PF
3.48	2.90	> 0.99	1.73	> 0.99	2.90	> 0.99
12.51	0.80	> 0.99	0.48	> 0.99	0.80	> 0.99

of $\mu = 0.0$ and $\mu = 1.0$ deteriorates as expected from the theory.

5.3 Three-Phase Shunt APF

Now, the three-phase shunt APF is simulated and its circuit schematics is depicted in Figure 5.8. It consists of a grid, modeled as an ideal three-phase voltage source, feeding a non-linear load of rated power of $10kW$, and a three-phase full-bridge converter working as a filter connected in shunt configuration. The control and modulation block receives the grid currents and DC-bus voltage and for some strategies, also the grid voltages are received, for by means of control and modulation, defining the switches gates signals for the converter.

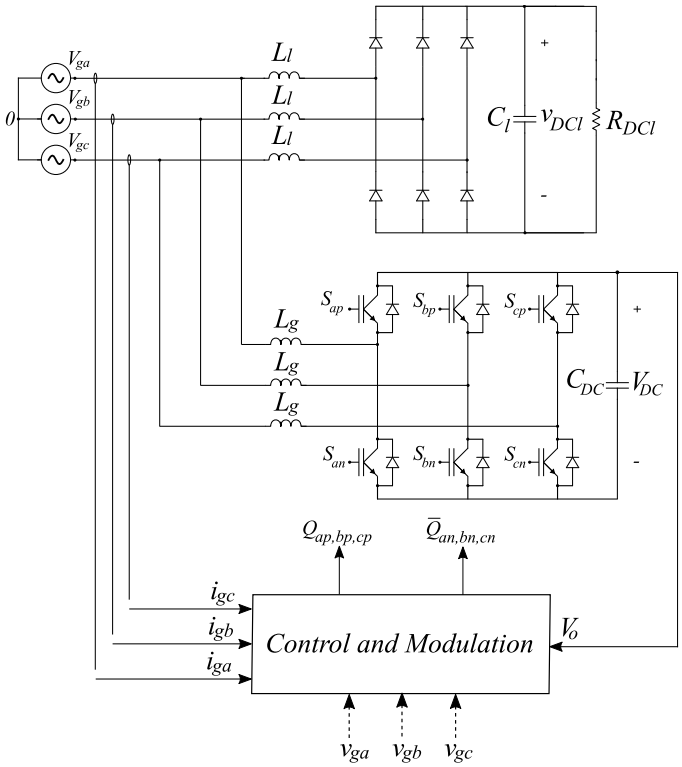


Figure 5.8: Circuit Schematics of Model of Medium Power Level Three-Phase Full-Bridge Shunt APF.

The parameterization of the system is done aiming to application of the control systems to industrial power level systems, with rated power of $10.0kW$.

Similarly to the PFC model studied in Section 5.2, the grid voltage is modeled as an ideal three-phase voltage source with $V_{gPEAK} = 392.0V$ and the inductance values were chosen $L_g = 1.22mH$ for $\lambda \approx 0.4$, $L_g = 3.48mH$ for $\lambda \approx 0.75$ and $L_g = 12.51mH$ for $\lambda \approx 0.9$.

The inductances L_g were chosen based on (4.22) obtaining $L_g = 3.48mH$ for $\lambda \approx 0.75$ and $L_g = 12.51mH$ for $\lambda \approx 0.9$, aiming to evaluate the system response with higher and lower inductance values.

with similar approach to that done in Section

The parameters are summarized in Table 5.3.

Table 5.7: Parameters for Simulations of Medium Power Level Three-Phase Shunt APF Model.

Parameter	Value
P	$10.0kW$
V_{gPEAK}	392.0 V
V_{DC}	1120.0 V
C_{DC}	$1.0mF$
L_L	$7.0mH$
C_L	$20.0\mu F$
R_L	37Ω
m	0.7
f_s	$30kHz$

The non-linear load phase current is shown in Figure 5.9. It has a PF of 0.899 and THD of 28.32%.

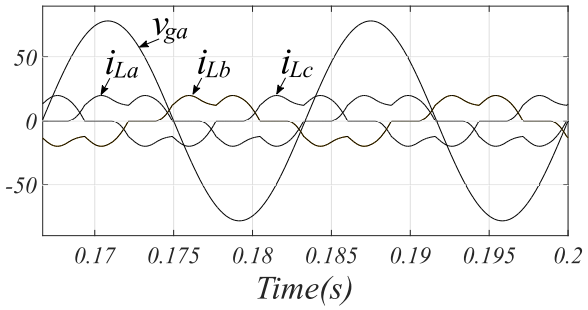


Figure 5.9: Simulation Results for Medium Power Level Three-Phase Shunt APF Model with Standard pq-PWM with PI Current Control - Phase voltage a (5 V/div.) and Phase Currents (1 A/div.): Non-Linear Load Current.

The performance of the system is comparatively analyzed for the control with Conventional pq-PWM and for DOCC strategies. The converter inductances L_g were chosen with values of $1.22mH$, $3.48mH$ and $12.51mH$, i.e., values smaller and bigger than load inductance L_L, with the objective to evaluate the influence of the ratio between filter inductance and load inductance on system performance.

5.3.1 Conventional pq-PWM

In Section 2.3 the conventional pq-PWM control for APF were presented. It consists of an extractor based on pq theory for calculation of harmonic and reactive content of load power to define the reference currents for the current controller. These control techniques performance depends on the speed and accuracy of the calculation of harmonic components of the non-linear loads and may demand high-speed microprocessors. Furthermore, the effectiveness of these techniques relies on the current controller performance.

5.3.1.1 Hysteresis Current Control

First, the system is controlled by Conventional pq-PWM with Hystersis Current Control and its results are shown in Figure 5.10 and Table 5.3.1.1.

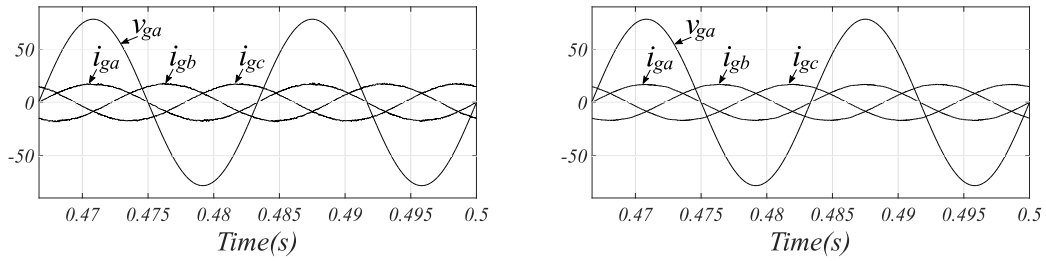


Figure 5.10: Simulation Results for Medium Power Level Three-Phase Shunt APF Model with Standard pq-PWM with Hysteresis Current Control - Phase voltage a (5 V/div.) and Phase Currents (1 A/div.): (a) $L_g = 3.48mH$, (b) $L_g = 12.51mH$.

Table 5.8: Simulation Results for Medium Power Level Three-Phase Shunt APF Model with DOCC with Standard pq-PWM with Hysteresis Current Control.

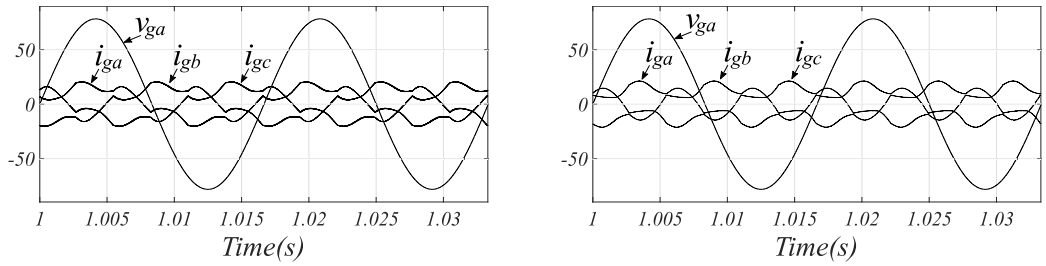
$L_g(mH)$	THD (%)	PF
1.22	8.29	> 0.99
3.48	2.10	> 0.99
12.51	1.19	> 0.99

It can be seen the PF close to unity for all the values of L_g, showing the effectiveness for reactive compensation. On THD, the strategy also showed good results for big and intermediary value of L_g. However for small value of L_g the result were deteriorated. This is due to lower filter capability and to high value of di/dt.

5.3.1.2 PI Current Control

First, the system is controlled by Conventional pq-PWM with Hystersis Current Control

Next, the system is controlled by Conventional pq-PWM with dq-PWM current controller in Figure 5.11, for $L_g = 3.48mH$ and $L_g = 12.51mH$. The values of PF and THD are summarized in Table 5.3.1.2.



(a) (b)

Figure 5.11: Simulation Results for Medium Power Level Three-Phase Shunt APF Model with Standard pq-PWM with PI Current Control - Phase voltage a (5 V/div.) and Phase Currents (1 A/div.): (a) $L_g = 3.48mH$, (b) $L_g = 12.51mH$.

Table 5.9: Simulation Results for Medium Power Level Three-Phase Shunt APF Model with DOCC with Standard pq-PWM with PI Current Control.

$L_g(mH)$	THD (%)	PF
1.22	16.69	0.98
3.48	21.43	0.96
12.51	30.42	0.95

It can be observed that the PF results have sensibility to converter inductance L_g, since a bigger inductance induces a bigger time constant for the system response. Concerning THD, the results showed insufficient performance of the system, showing PI controllers are inadequate for this application, because of its reduced control bandwidth.

5.3.2 DOCC

The simulations of three-phase shunt APF are then carried out with DOCC with grid voltage measurement for four different values of k. From (4.40), (4.29), (4.50) the equivalent resistance and minimum value of converter inductance for each case are listed:

- $k = 0$ (standard OCC): $R_e = 23.05\Omega$, $L > 326.54\mu H$;
- $k = 0.0217$ (50% faster): $R_{es} = 46.10\Omega$, $L > 653.08\mu H$;
- $k = 0.0108$ (25% faster): $R_{es} = 30.73\Omega$, $L > 435.39\mu H$;
- $k = -0.0108$ (25% slower): $R_{es} = 18.44\Omega$, $L > 261.23\mu H$.

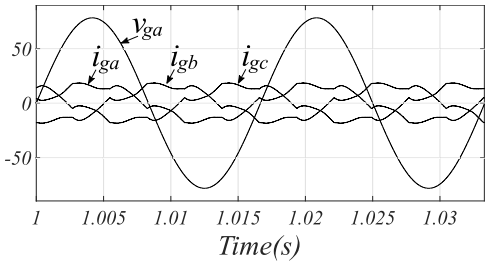


Figure 5.12: Simulation Results for Medium Power Level Three-Phase Shunt APF Model with DOCC - Phase voltage a (5 V/div.) and Phase Currents (1 A/div.): (a) $L_g = 3.48mH$, (b) $L_g = 12.51mH$.

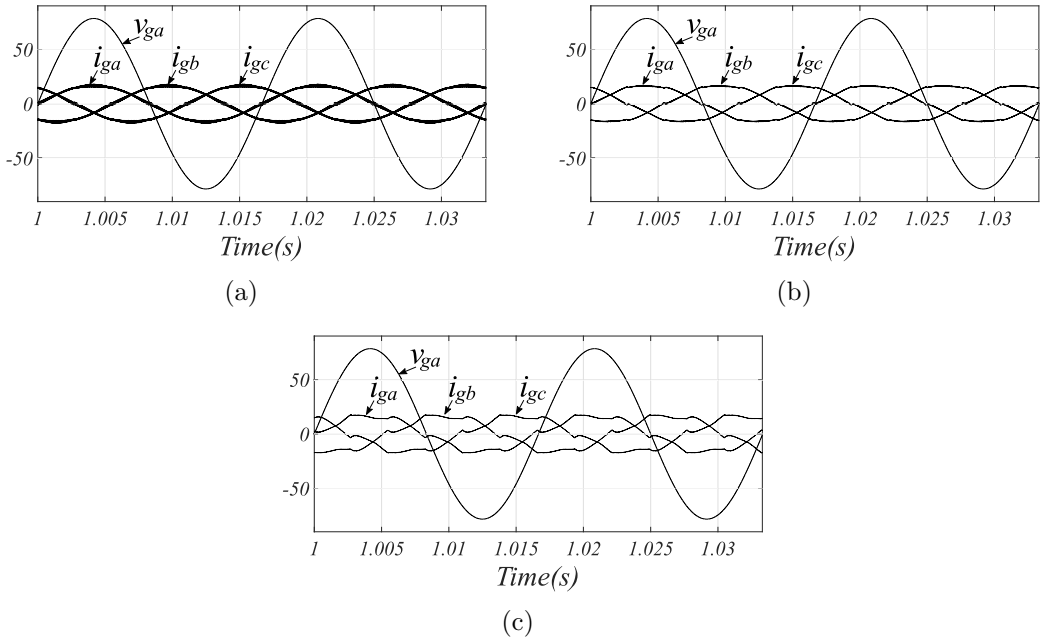
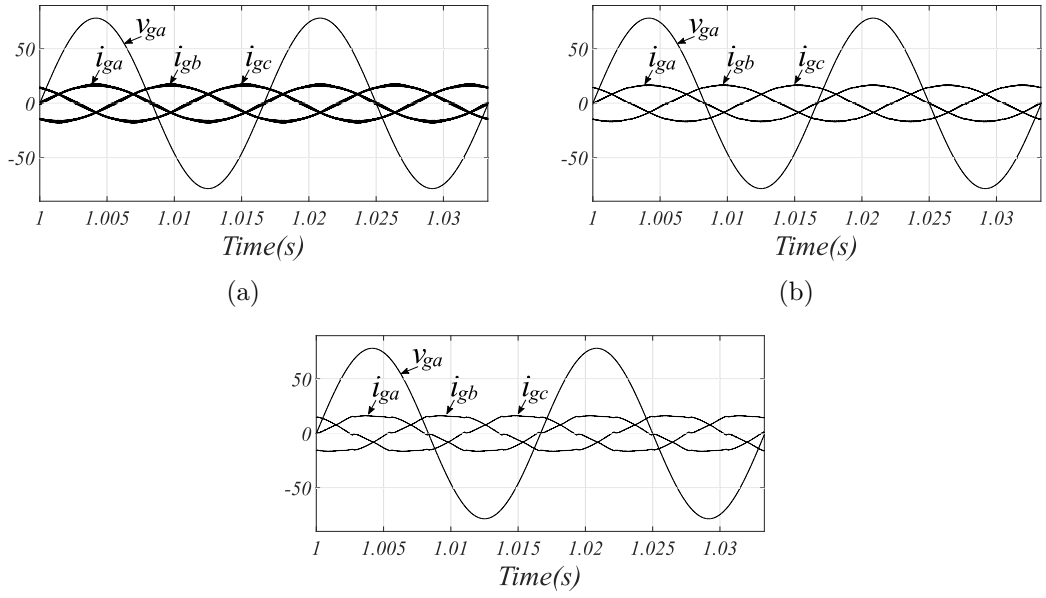


Figure 5.13: Simulation Results for Medium Power Level Three-Phase Shunt APF Model with DOCC With Grid Voltage Measurement for $k = 0.0159$ (faster) - Phase voltage a (5 V/div.) and Phase Currents (1 A/div.): (a) $L_g = 3.48mH$, (b) $L_g = 12.51mH$.

The results are shown in Figures 5.12-5.15 and Tables 5.3.2-5.3.2.

From Figures 5.12-5.15 and Tables 5.3.2-5.3.2, it can be seen that PF have influence of inductance L_g, an inherent characteristic of OCC-based methods. Besides, harmonic filtering performance is strongly related to L_g. It can be observed that in the case of inductance $L = 1.22mH$ small content of low order harmonics are obtained but with significant high order content. When the inductance value is increased to $L = 12.51mH$ there is an improvement on the content of high order harmonics however with a deterioration on the low order harmonics and degradation of PF.

Analyzing each line of 5.3.2, i.e., fixing a inductance, it can be seen that the best results regarding PF and THD are for $k > 0$ and the worst for $k < 0$, since gain k modifies the dynamics response of current control, as extensively shown throughout



(a) (b)

(c)

Figure 5.14: Simulation Results for Medium Power Level Three-Phase Shunt APF Model with DOCC With Grid Voltage Measurement for $k = 0.0317$ (faster) - Phase voltage a (5 V/div.) and Phase Currents (1 A/div.): (a) $L_g = 3.48mH$, (b) $L_g = 12.51mH$.

Table 5.10: Simulation Results for Medium Power Level Three-Phase Shunt APF Model with DOCC.

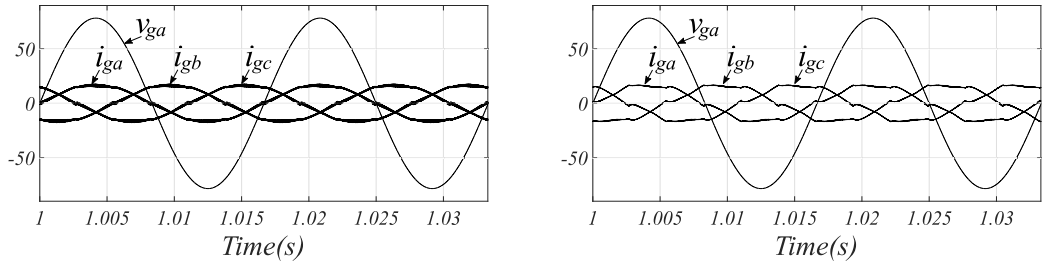
L_g	THD(%)	PF
1.22 (mH)	5.62	0.9984
3.48 (mH)	8.11	0.9967
12.51 (mH)	20.95	0.9788

this work. Overall, the best results are obtained for $k = 0.0217$ (50% faster) and $L_g = 3.48mH$ an intermediary inductance. The worst results are achieved with $k = -0.0180$ (25% slower) and $L_g = 12.24mH$.

5.3.3 Comparative Analysis

From the point of view of control complexity, the DOCC brings a very simple implementation, with only one PI controller for DC bus voltage and the current control being realized together with PWM modulation. This technique could be applied by low-cost microprocessor since the number of A/D conversion is minimal and calculations related to the control technique are reduced.

For PFC Rectifier, compared to conventional dq-PWM control the performance on harmonics filtering with DOCC strategies are on the same order of magnitude. Concerning PF the dq-PWM garantees close to unity PF, what is not guaranteed by DOCC without a strategy for compensation of inductive voltage drop.



(a) (b)

Figure 5.15: Simulation Results for Medium Power Level Three-Phase Shunt APF Model with DOCC With Grid Voltage Measurement for $k = -0.0159$ (slower) - Phase voltage a (5 V/div.) and Phase Currents (1 A/div.): (a) $L_g = 3.48mH$, (b) $L_g = 12.51mH$.

Table 5.11: Simulation Results for Medium Power Level Three-Phase Shunt APF Model with DOCC with Grid Voltage Measurement.

	$k = 0.0217$		$k = 0.0180$		$k = -0.0180$	
$L_g(mH)$	THD(%)	PF	THD(%)	PF	THD(%)	PF
1.22	5.02	0.9987	5.20	0.9986	6.21	0.9981
3.48	2.64	0.9997	5.27	0.9986	10.79	0.9942
12.51	6.90	0.9976	15.40	0.9883	24.24	0.9719

The DOCC technique with voltage measurement brings a bit more of complexity, since there are more sensors (phase voltage sensors). However, the technique has much effect on PF and current dynamic response. The steady state results of the DOCC with voltage measurement are equivalent to dq-PWM for $k > 0$.

The inductive drop compensation has shown excellent results of PF correction, and avoids the use of voltage sensors. However, compared to DOCC this technique requires more computational resources and may be not suitable for some low cost microprocessor-based devices.

For shunt APF, DOCC strategies showed the best results for $k > 0$ and an intermediary inductance value L_g. In fact, the inductance has strong influence on the filter dynamics because of its filtering effect. For high values of inductance the high order harmonics content is diminished, however for low order harmonics the filter has low effectiveness, and vice-versa. It is therefore important to have some knowledge about the load on dealing with the filter design.

The pq extractor methods analyzed are more complex in their control structure itself and demands more sensors on their implementation: current sensors for load and converter, and voltage sensors for the grid. The pq with PI current control technique has shown unsatisfactory results concerning THD, as expected. The hysteresis current control has the best results but has intrinsic drawbacks of dead zones for input current close to zero and variable switching frequency.

5.4 Partial Conclusions

In this chapter the simulation results of PFC rectifier and APF have been shown and analyzed. The control methods for PFC were the DOCC strategies and the conventional dq-PWM method. For the APF the DOCC strategies were also applied and the pq extractor-based control methods were also applied.

DOCC has very simple structure and has very good results in PFC Rectifier and shunt APF applications, with results comparable to conventional PWM methods. The intrinsic drawback of inductive voltage drop can be compensated with feed-forward compensation with improved computational effort. Furthermore HPWM can be incorporated to DOCC.

Chapter 6

Model Validation and Experimental Results

6.1 Introduction

The three-phase PFC Rectifier and APF systems are then implemented in simulations carried out in PSIM environment and in experimental setup to validate the system modeling and applicability of the control strategies studied throughout this work.

The available devices on Laboratory allows the experimental power circuit topologies to be in the scale of dozens of Watts. Therefore, to permit an adequate comparation with the medium scale system analyzed in Chapter 5 the parameterization of the power circuit topologies of the systems analyzed in this Chapter are scaled down.

6.2 Low Power Level Setup

For experimental validation of the system it will be used a three-phase full-bridge converter BOOSTXL-DRV8305EVM from Texas Instruments [116] with maximum operating DC-link voltage of $45.0V$. Therefore the maximum synthesizable AC voltage with converter operation in linear modulation range ($m \leq 1.0$) can be defined as

$$V^*_{g_{MAX}} = \frac{m}{2} V_{DC}\Big|_{\substack{m=1.0 \\ V_{DC}=45.0}} = 22.5V. \tag{6.1}$$

Since the available phase grid voltage amplitude on laboratory is 179.6 V ($127V_{RMS}$) the synthesized voltages by the converter on AC side must be conditioned to grid level which can be done by means of an arrangement of three single

phase transformers with 16 : 127 turns ratio connected in star–delta (Y-D), as illustrated in Figure 6.1, hence providing a $16/\sqrt{3} : 127$ turns ratio.

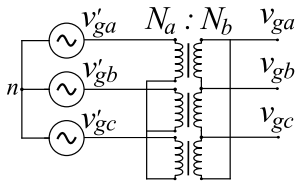


Figure 6.1: Three-Phase Step-up Transformer Arrangement for Low Scale Setup.

Therefore, with the connection of arrangement of 6.1 with the lab grid, the phase voltage on converter side will be

$$v_g = 13.06V. \tag{6.2}$$

The circuit schematics of low scale models of three-phase PFC and shunt APF are shown in Figure 6.2: the PFC Rectifier circuit schematics, in Figure 6.2-(a), consists of a grid modeled as an ideal three-phase voltage source connected to a step-down three-phase transformer, and three-phase full-bridge converter with the DC load modeled as a Resistor R_{DC}. The shunt APF circuit schematics depicted in Figure 6.2-(b) is made up with the same grid-transformer arrangement as the PFC Rectifier, but in this case supplying a non-linear load, and a three-phase full-bridge converter connected in shunt working as APF.

Circuit Schematics of Medium Power Level Three-Phase Full-Bridge PFC Rectifier Model.

The parameterization of the converter is done now. The available DC load was $R_{DC} = 21.3\Omega$. The inductance values of the systems analyzed in Chapter 5 are scaled down based ok keeping the same duty-cycle convergence ratio μ according to (4.22) obtaining:

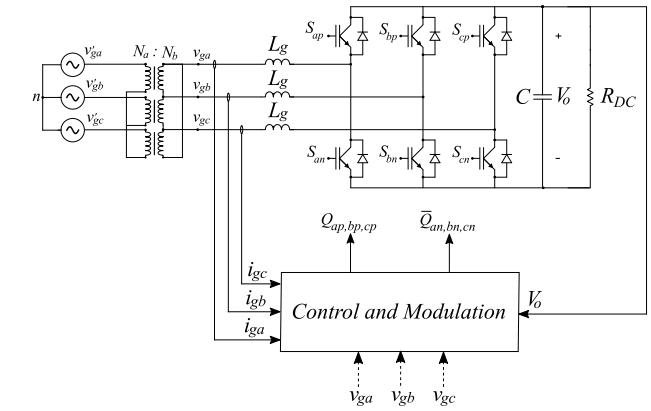
- PFC Rectifier

$$L_{g1} = 600\mu H;$$
$$L_{g2} = 2.13mH.$$

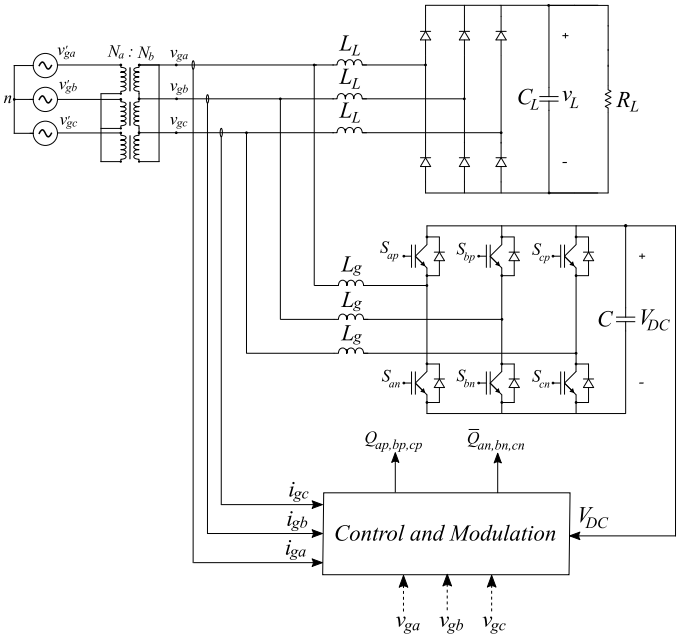
- Shunt APF

$$L_{g1} = 300\mu H;$$
$$L_{g2} = 600\mu H;$$
$$L_{g3} = 2.13mH.$$

The converter capacitor, as seen in Chapter 4, has no influence on current control dynamics, so that its value kept the same from medium power scale system, i.e.



(a)



(b)

Figure 6.2: Circuit Schematics of Medium Power Level Three-Phase Models: (a) Full-Bridge PFC Rectifier, (b) Shunt APF.

$$C = 1mF.$$

The main parameterization for both circuits are summarized in Table 6.2.

6.3 Simulations

The three-phase PFC Rectifier and APF systems illustrated in Figure 6.2 are now studied through simulations in PSIM environment with standard PWM and DOCC strategies. The performance of these systems with such control strategies at this power level will be characterized by analysis of steady-state results regarding PF and THD, and will be compared to those obtained in medium power level simulations

Table 6.1: Parameters for Simulations of Low Power Level Three-Phase Full-Bridge PFC Rectifier and Shunt APF Models.

Parameter	PFC	APF
P	$72W$	$21.4W$
v_g	$13.06V$	$13.06V$
V_{DC}	39.2 V	39.2 V
m	0.67	0.67
f_s	$30kHz$	$30kHz$
C_{DC}	340.0μ F	340.0μ F
R_{DC}	21.3Ω	—
R_L	—	21.3Ω
L_L	—	1.0 mH
C_L	—	$340.0\mu F$

shown in Chapter 5.

6.3.1 Three-Phase PFC

First, the three-phase PFC rectifier controlled by standard dq-PWM and DOCC strategies is simulated and the steady-state results are shown in the following subsections.

6.3.1.1 dq-PWM Control

The standard dq-PWM technique is applied to the three-phase PFC rectifier and the results are shown in Table 6.2.

Table 6.2: Simulation Results for Low Power Level Three-Phase Full-Bridge PFC Rectifier Model with Standard dq-PWM.

L_g	$600\mu H$	$2.13mH$
THD	1.72	0.49
PF	> 0.99	> 0.99

It can be seen from the results that the PF is approximately unitary for both inductance values and the THD results are low. In fact, comparing Table 6.2 to 5.2.2, it can be seen the results are quite similar, obviously showing the technique is suitable for medium and low power level applications.

6.3.1.2 DOCC

The simulations are then carried out with DOCC strategies, similarly to the methodology applied in Chapter 5. The results for DOCC strategy with only current sensing for $L_g = 600\mu H$ and $L_g = 2.13mH$ are shown in Table 6.3.

Table 6.3: Simulation Results for Low Power Level Three-Phase Full-Bridge PFC Rectifier Model with DOCC Grid with Voltage Measurement.

	k = 0.0		k = 0.15		k = -0.15	
L_g (mH)	THD	PF	THD	PF	THD	PF
0.6	1.78	0.99	1.78	> 0.99	1.78	> 0.99
2.13	0.48	0.98	0.50	> 0.99	0.46	0.95

It can be seen that the inductance has much influence on steady-state harmonics and PF, furthermore use of grid voltage sensing signals has less influence on THD and much on PF, similarly to those results obtained in Chapter 5.

Following, the results for DOCC with Feed-forward inductive voltage drop compensation are shown in Table 6.3.1.2 for $L_g = 600\mu H$ and $L_g = 2.13mH$.

Table 6.4: Simulation Results for Low Power Level Three-Phase Full-Bridge PFC Rectifier Model with DOCC with Feed-forward Inductive Voltage Drop Compensation.

L_g (mH)	THD	PF
0.6	1.78	> 0.99
2.13	0.5	> 0.99

The correction of inductive voltage drop has shown satisfactory results at this power level, with the PF for both inductances close to unity, similarly to those results obtained in Chapter 5.

The results of PF and THD for the PFC Rectifier controlled by DOCC with Saddle PWM for $L_g = 600\mu H$ are shown in Table 6.5.

Table 6.5: Simulation Results for Low Power Level Three-Phase Full-Bridge PFC Rectifier Model with DOCC with Hybrid PWM.

μ	THD (%)	PF
0.0	2.81	> 0.99
0.5	1.66	> 0.99
1.0	2.81	> 0.99

Again, the application of $\mu = 0.5$ improves the THD, while $\mu = 0.0$ and $\mu = 1.0$ deteriorates. On the other hand, the variation of μ has minor influence on PF. These results corroborates those obtained in Chapter 5.

6.3.2 APF

Now, the three-phase shunt APF controlled with standard pq-PWM and DOCC strategies is simulated and the steady-state results are shown subsequently.

6.3.2.1 pq-PWM Control

The standard pq-PWM technique is applied to three-phase shunt APF for $L_g = 600\mu H$ and $L_g = 2.13mH$ with hysteresis and with dq-PWM current controllers. The results are shown in Table 6.6.

Table 6.6: Simulation Results for Low Power Level Three-Phase Shunt APF Model with Standard pq-PWM with Hysteresis and PI Current Controls.

	Hysteresis		PI	
L_g (mH)	THD(%)	PF	THD(%)	PF
0.6	1.34	>0.99	22.22	0.99
2.13	1.30	>0.99	36.65	0.99

It can be seen the PF close to unity for all the values of L_g, showing the effectiveness for reactive compensation. On THD, the strategy also showed good results for big and intermediary value of L_g. However for small value of L_g the result were deteriorated. This is due to lower filter capability and to high value of di/dt.

It can be observed that the PF results have sensibility to converter inductance L_g, since a bigger inductance induces a bigger time constant for the system response. Concerning THD, the results showed insufficient performance of the system, showing PI controllers are inadequate for this application, because of its reduced control bandwidth.

6.3.2.2 DOCC

Similarly to the procedure done in Chapter 5, the simulations are carried with DCC strategies for four different values of k. The equivalent resistance and minimum value of converter inductance for each case are listed:

- $k = 0$, standard DOCC: $R_e = 11.75\Omega$, $L_g > 166.46\mu H$;
- $k = 0.04$ (50% faster): $R_{es} = 22.17\Omega$, $L_g > 314.07\mu H$;
- $k = 0.02$ (25% faster): $R_{es} = 15.36\Omega$, $L_g > 217.59\mu H$;
- $k = -0.02$ (25% slower): $R_{es} = 9.51\Omega$, $L_g > 134.78\mu H$.

The results are shown in Table 6.7. Again, it is explicit the influence of inductance L_g and of gain k on PF. The best results are obtained for $k = 0.04$ (50% faster) and intermediary inductance $L_g = 600\mu H$, similarly to Chapter 5.

6.4 Experimental

The systems are then experimentally implemented with standard PWM and DOCC strategies for PFC Rectifier; and DOCC strategies for APF. Steady-state results

Table 6.7: Simulation Results for Low Power Level Three-Phase Shunt APF Model with DOCC with Voltage Measurement.

	k = 0.0		k = 0.02		k = 0.04		k = -0.02	
L_g (mH)	THD(%)	PF	THD(%)	PF	THD(%)	PF	THD(%)	PF
0.3	11.62	0.99	11.53	0.99	–	–	11.75	0.99
0.6	7.74	1.0	6.99	1.0	6.34	1.0	8.61	1.0
2.13	17.39	0.99	13.72	0.99	13.72	0.99	20.76	0.98

regarding PF and THD will be brought to characterize the performance of these control strategies on each system.

6.4.1 PFC

The three-phase PFC rectifier controlled by standard dq-PWM and DOCC strategies are experimentally implemented and the steady-state results are shown in the afterwards.

6.4.1.1 dq-PWM Control

The results for the PFC controlled with conventional dq-PWM control for $L = 600\mu H$ and $L = 2.13mH$ are shown in Figure 6.3 and Table 6.8.

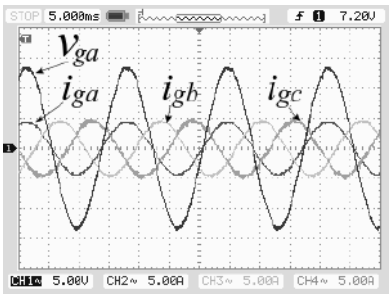


Figure 6.3: Experimental Results Low Power Level Three-Phase Full-Bridge PFC Rectifier with Standard dq-PWM Control - Phase voltage a (5 V/div.) and Phase Currents (5 A/div.): $L_g = 600\mu H$.

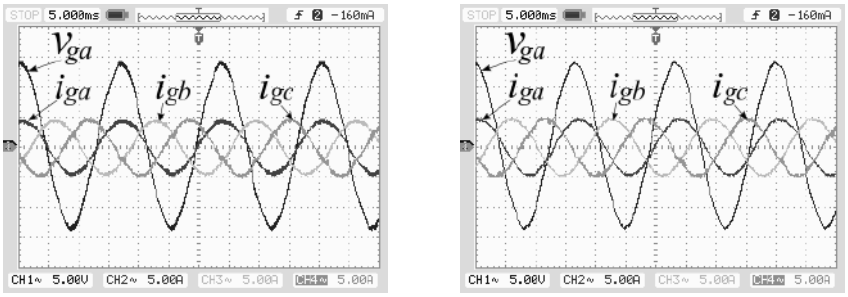
Table 6.8: Experimental Results for Low Power Level Three-Phase Full-Bridge PFC Rectifier Model with Standard dq-PWM Control.

L_g (mH)	THD(%)	PF
0.6	4.78	> 0.99
2.13	3.23	> 0.99

These results are similar compared to those obtained from simulations of low scale model. It can be seen that the PF is almost unitary for both inductances, and the best results are achieved with bigger L_g.

6.4.1.2 DOCC Strategies

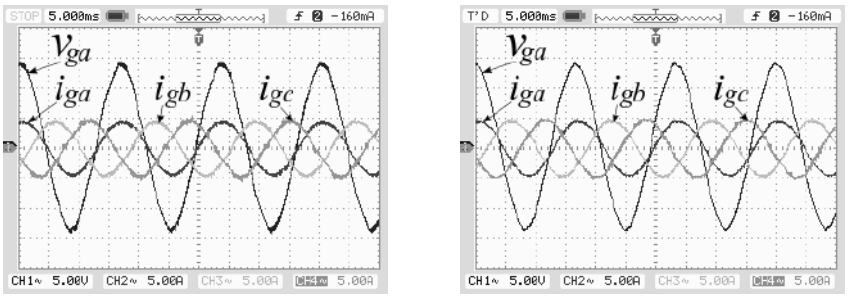
First, the results for steady state operation for the PFC Rectifier controlled by DOCC with only current sensing for $L_g = 600\mu H$ and $L_g = 2.13mH$ are shown in Figure 6.4 and the first column of Table 6.9.



(a) (b)

Figure 6.4: Experimental Results Low Power Level Three-Phase Full-Bridge PFC Rectifier with DOCC - Phase voltage a (5 V/div.) and Phase Currents (5 A/div.): (a) $L_g = 600\mu H$., (b) $L_g = 2.13mH$.

The results for steady state operation of the PFC Rectifier controlled by DOCC grid voltage measurement with $k > 0$ for $L_g = 600\mu H$ and $L_g = 2.13mH$ are shown in Figure 6.5.



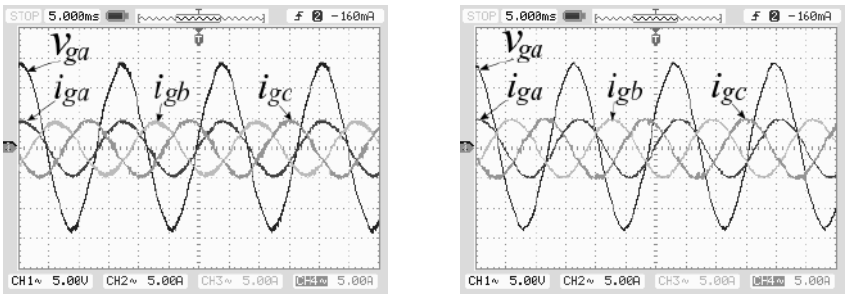
(a) (b)

Figure 6.5: Experimental Results Low Power Level Three-Phase Full-Bridge PFC Rectifier with DOCC with Grid Voltage Measurement for $k = 0.015$ (faster)- Phase voltage a (5 V/div.) and Phase Currents (5 A/div.): $L_g = 600\mu H$.

Next, the results are shown for $k < 0$ for $L_g = 600\mu H$ and $L_g = 2.13mH$ in Figures 6.6 and 6.7.

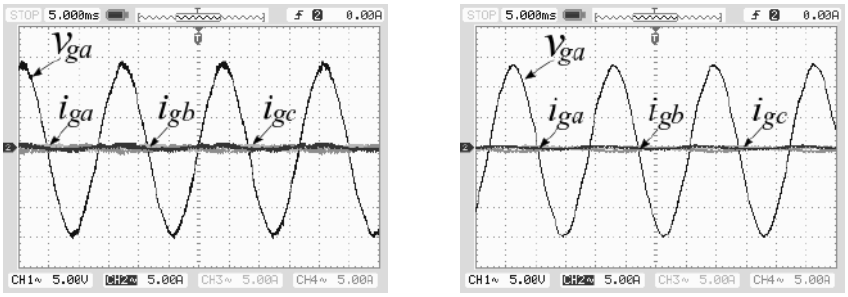
The results for DOCC with voltage measurement are summarized in Table 6.9.

For DOCC with only grid current sensing and DOCC with grid voltage measurement it is explicit the influence of the converter input inductance on the results. From the results with $k > 0$, the currents exhibit a slightly bigger THD, but still close to 5% in both cases. This can be due to noise in voltage measurements which brings increase in harmonic content of the modulation signal. On the other hand,



(a) (b)

Figure 6.6: Experimental Results Low Power Level Three-Phase Full-Bridge PFC Rectifier with DOCC with Grid Voltage Measurement for $k = -0.015$ (slower) - Phase Voltage a (5 V/div.) and Phase Currents (5 A/div.): (a) $L_g = 600\mu H$, (b) $L_g = 2.13mH$.



(a) (b)

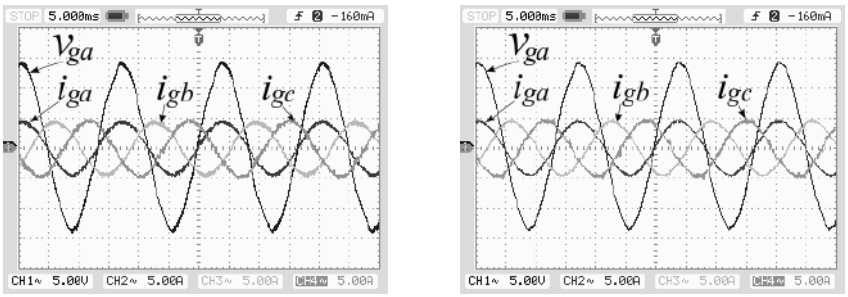
Figure 6.7: Experimental Results Low Power Level Three-Phase Full-Bridge PFC Rectifier with DOCC with Grid Voltage Measurement for $k = -0.015$ (slower) at null load operating point - Phase Voltage a (5 V/div.) and Phase Currents (5 A/div.): (a) $L_g = 600\mu H$, $L_g = L_g = 2.13H$.

as expected, the PF increased. The currents for $k < 0$ have THD in the same level, but the PF results are degraded. Furthermore, it can be seen the operation at null load is allowed, with some parasitic current flowing only to supply the resistances of the circuit and losses of the converter.

The results for the converter controlled with OCC and with compensation of inductive drop are shown in Figure 6.8. As it can be seen, the technique does not have much influence on the harmonics but has a very good effectiveness on the correction of PF.

Table 6.9: Experimental Results for Low Power Level Three-Phase Full-Bridge PFC Rectifier Model with DOCC with Voltage Measurement.

	k = 0.0		k = 0.15		k = -0.15	
L_g (mH)	THD	PF	THD	PF	THD	PF
0.6	4.86	0.98	5.11	0.98	5.15	0.75
2.13	3.75	0.84	3.91	0.91	3.51	0.99



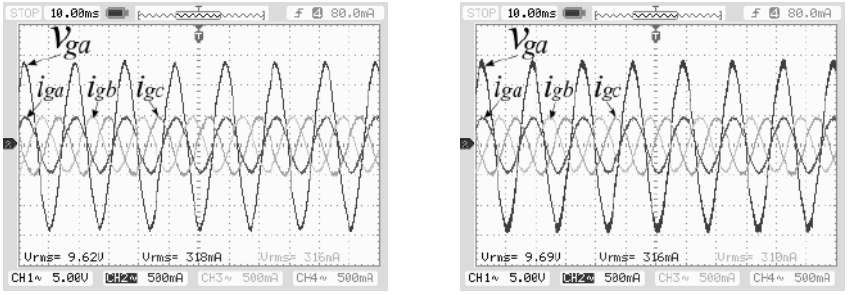
(a) (b)

Figure 6.8: Experimental Results Low Power Level Three-Phase Full-Bridge PFC Rectifier with DOCC with Feed-forward Inductive Drop Compensation - Phase voltage a (5 V/div.) and Phase Currents (5 A/div.): $L_g = 600\mu H$.

Table 6.10: Experimental Results for Low Power Level Three-Phase Full-Bridge PFC Rectifier with DOCC with Feed-forward Inductive Voltage Drop Compensation.

$L_g\ (mH)$	THD(%)	PF
0.6	3.91	> 0.99
2.13	5.45	> 0.99

DOCC with Hybrid PWM technique is implemented and the results are shown in 6.9-6.10. The best results concerning THD are those with $\mu = 0.5$. However, with $\mu = 0.99$ even though the THD deteriorates, the switching losses are expected to be reduced by 33%.

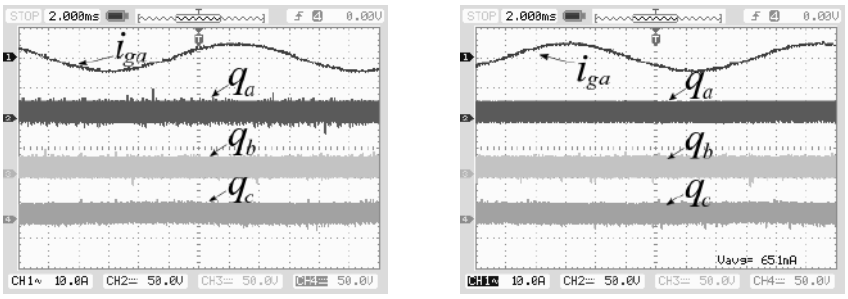


(a) (b)

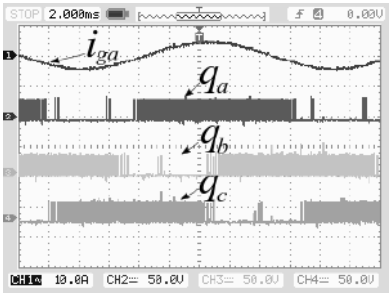
Figure 6.9: Experimental Results Low Power Level Three-Phase Full-Bridge PFC Rectifier with DOCC with Hybrid PWM - Phase voltage a (5 V/div.) and Phase Currents (5 A/div.): (a) $\mu = 0.5$, (b) $\mu = 0.99$.

6.4.2 Three-Phase Shunt APF

The non-linear-load currents are shown in Figure 6.11, whose The THD of the line currents drawn from this load is of 24.79%.



(a) (b)



(c)

Figure 6.10: Experimental Results Low Power Level Three-Phase Full-Bridge PFC Rectifier with DOCC with Hybrid PWM - Phase Current a (10 A/div.) and Switch Gating Signals (5 V/div.): (a) Conventional, (b) $\mu = 0.5$, (c) $\mu = 0.99$.

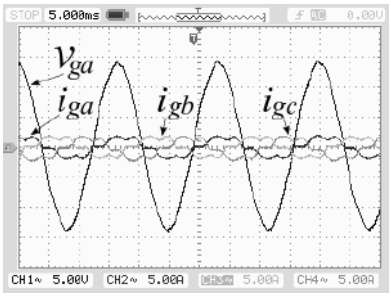


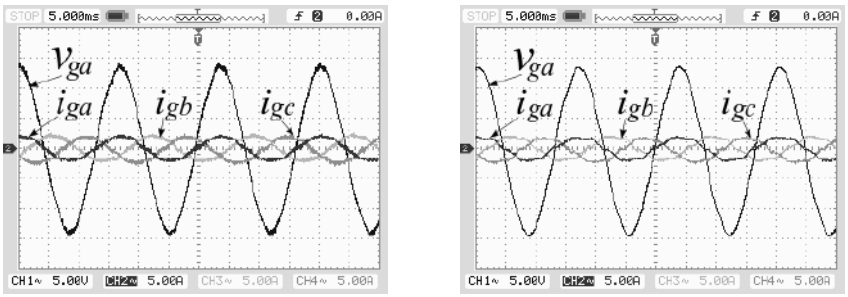
Figure 6.11: Experimental Results non-linear load without APF: Grid Phase Voltage a (5 V/div.) and Grid Phase Currents (5 A/div.).

6.4.2.1 DOCC Strategies

The results for APF with DOCC with only current sensing for $L = 600\mu H$ and $L = 2.13mH$ are shown in Figure 6.12.

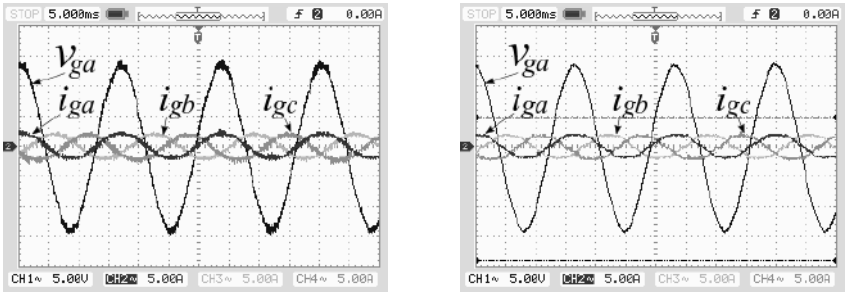
The results for APF with DOCC with grid voltage measurement for $k = 0.05$ (faster) with $L_g = 600\mu H$ and $L_g = 2.13mH$ are shown in Figure 6.13.

The results for APF with DOCC with $k = -0.594667$ (slower) with $L_g = 600\mu H$ and $L_g = 2.13mH$ are shown in Figure 6.14.



(a) (b)

Figure 6.12: Experimental Results Low Power Level Three-Phase Shunt APF with DOCC - Phase Voltage a (5 V/div.) and Phase Currents (5 A/div.): (a) $L_g = 600\mu H$, (b) $L_g = 2.13mH$.



(a) (b)

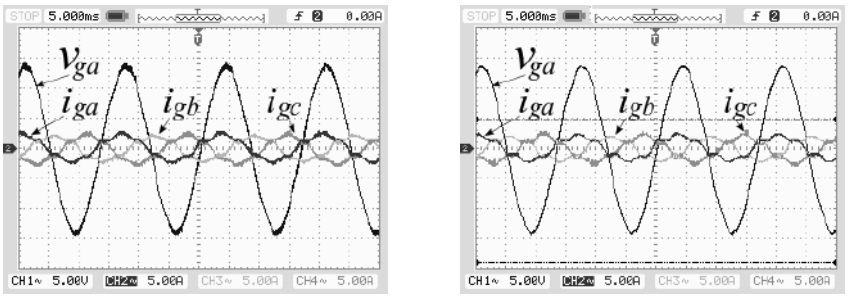
Figure 6.13: Experimental Results Low Power Level Three-Phase Shunt APF with DOCC with Grid Voltage Measurement for $k = 0.05$ (faster)- Phase Voltage a (5 V/div.) and Phase Currents (5 A/div.): (a) $L_g = 600\mu H$, (b) $L_g = 2.13mH$.

6.5 Analysis

Comparing the results from Tables 6.2,6.3 from simulation results and 6.8, 6.9 from experimental results it can be seen that the DOCC with only current sensing and the standard PWM-dq strategies have equivalent results, with the dq-PWM slightly better for both THD and PF performance.

For DOCC with voltage measurement, the results confirms improvements on PF with $k > 0$ and deterioration with $k < 0$. The improvements on THD for $k < 0$ determined in theory and found in simulations has been observed only for $L_g = 2.13mH$ in experimental results, what indicates the presence of saturation and parasitic effects in the inductor of $L_g = 600\mu H$. Furthermore, the results from Figure 6.7 verifies that the null operation is allowed for $k < 0$.

The results from Table 6.4.1.2 shows that the inductive voltage drop is fully compensated, with the PF close to unity for both inductance values. However, the THD has damaged, what was not predicted. Even though the quadrature current is filtered, the gain by which this current is multiplied to estimate the inductive voltage drop is function of the measured DC-bus voltage as well as of the output of the



(a) (b)

Figure 6.14: Experimental Results Low Power Level Three-Phase Shunt APF with DOCC with Voltage Measurement with $k = -0.594667$ (slower) - Phase Voltage a (5 V/div.) and Phase Currents (5 A/div.): (a) $L_g = 600\mu H$, (b) $L_g = 2.13mH$.

Table 6.11: Experimental Results for Low Power Level Three-Phase Shunt APF with DOCC with Grid Voltage Measurement.

	k = 0.0		k = 0.025		k = 0.05		k = -0.025	
L_g (mH)	THD	PF	THD	PF	THD	PF	THD	PF
0.6	11.70	> 0.99	11.34	> 0.99	11.71	> 0.99	11.63	0.99
2.13	13.73	> 0.99	11.91	> 0.99	10.81	> 0.99	13.72	> 0.99

DC-bus voltage regulator, where both have harmonic components. Therefore, the estimation of the inductive voltage drop to be compensated degrades the operation of the PFC Rectifier.

The APF controlled by DOCC with only current sensing has shown effectiveness on harmonics and reactive correction. The PF for both inductances values were close to unity, showing the effectiveness of this technique for PF correction. The current THD has decreased approximately 50% in real implementation for two both inductance values. Compared to simulation results it an be seen that $L_g = 600\mu H$ the experimental results are worse than simulation concerning THD but for $L_g = 2.13mH$ the experimental results are improved. This behavior can be due the supposed presence of saturation and parasitic effects in the inductor of $L_g = 600\mu H$.

For APF applications, from analysis of Table 6.4.2.1 the use of $k > 0$ shows improvements on active filtering capabilities. The results show efficient PF correction. Quantitatively, the improvements on THD were more sensitive for $L_g = 2.13mH$. Since k enlarges dynamic response, therefore the cut-off frequency of current control is enlarged, and a bigger L_g filters high order harmonics, the results evidences this strategy works well for intermediary inductance values. The use of $k < 0$ is not interesting about filtering capability, since it deteriorates THD. Its use would be justified for null load operation, so that a dynamic k would be applicable.

6.6 Partial Conclusions

In this chapter simulation and experimental results of low power level PFC rectifier and APF with standard PWM and DOCC strategies have been shown and analyzed.

DOCC strategies has presented to be very suitable for applications in three-phase PFC and shunt APF systems. Furthermore, the similar behavior among medium and low power levels simulations and experimental results reveals induced the applicability of these strategies to medium power level applications.

Chapter 7

General Conclusions and Future works

In this work it has been studied the application of a digital strategy of OCC (DOCC) for the two main approaches for active PF and harmonics content correction: PFC Rectifier and Active Power Filtering.

Concerning the three-phase full-bridge PFC rectifier, DOCC with grid voltage measurement has shown equivalent results compared to standard dq-PWM control regarding PF and THD but with simpler implementation. DOCC has a very simple structure, with only one explicit controller, for the DC-bus voltage, since this strategy realizes simultaneously PWM modulation and current control. The use of grid voltage sensing signals has improved the PF and THD results at steady state. Moreover, a modification in the algorithm of feed-forward inductive voltage drop compensation has been proposed and tested, showing its improvement in PF correction.

The three-phase shunt APF with DOCC with voltage measurement has shown good performance with PF and harmonics compensation, making the PF to be close to unity and reducing the THD to approximately 50% of non compensated one. The use of voltage measurements has in fact improved the harmonic compensation capability of the APF, as expected by theoretical analysis in this work.

Also, the Hybrid PWM has been incorporated to DOCC, introducing a new variable so-called common mode modulation signal m_{N0}, to improve the performance of output voltage synthesis and DC-bus utilization. Besides, for an appropriate choice of the zero vector apportion ratio μ THD or power losses can be improved.

Finally, the stability analysis of OCC with triangular carrier has been carried out with Poincaré Maps Approach. It has been analytically derived the expression for mininum inductance value for duty-cycle convergence, showing that the use of triangular carrier enhances the stability of OCC when compared to sawtooth carrier.

For future works the following topics are listed:

1. Varying grid voltage measurement gain k: to adjust k according to the load, aiming optimal dynamics response. In this case, bidirectional converter topologies, the converter could operate in AC-DC and DC-AC conversions;

2. Application of the technique to low cost microprocessor-based devices, to evaluate its feasibility and limitations on selected devices;

3. Application of sampled-data modeling for the converter controlled by DOCC strategies for study of stability analysis of DOCC;

4. Design of DC-bus controller with discrete-time methods;

5. Feed-forward Compensation of inductive voltage drop, once grid voltage measurement is available, based on controlling the instantaneous reactive power to be zero, setting the amplitude of the quadrature current to be added to make up the modulation signal.

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Appendix A

Standards

A.1 European Standard EN 61000-3-2

Given an electronic or electrical equipment, it is necessary to define if the Standard is applicable to it or not. If so, the equipment is then classified in one of the four classes. The flow chart on Figure A.1 can be derived.

The limits of harmonics of each order are specified in Table A.1. The limits for equipments of classes A and B are determined as absolute values for each order, while the limits for class C equipments are percentual values of the fundamental component and for class D each harmonics limit is relative to total power of the equipment.

Table A.1: European Standard EN 61000-3-2: Harmonics Limits for Equipment Classes

Harmonics (n)	Class A	Class B	Class C	Class D
	Limit (A)	Limit (A)	Limit (% of fund.)	Limit (mA/W)
		Odd harmonics		
3	2.30	3.45	30xp.f.	3.4
5	1.14	1.71	10	1.9
7	0.77	1.155	7	1.0
9	0.40	0.60	5	0.5
11	0.33	0.495	3	0.35
13	0.21	0.315	3	3.85/13
$15 \leq n \leq 39$	0.15x15/n	0.225x15/n	3	3.85/n
		Even Harmonics		
2	1.08	1.62	2	-
4	0.43	0.645	-	-
6	0.30	0.45	-	-
$8 \leq n \leq 50$	0.23x8/n	0.345x8/n	-	-

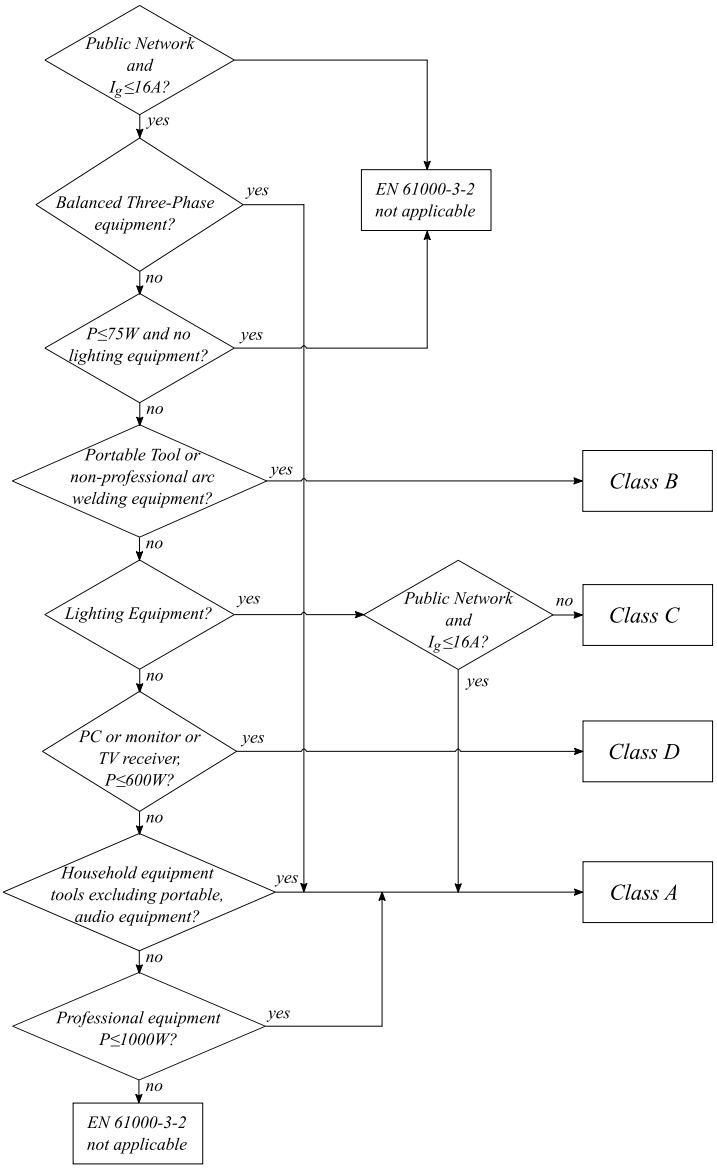


Figure A.1: Flow Chart for Classification of Electrical Equipment according to Standard EN 61000-3-2.

A.2 IEEE 519-2014

The recommendations from the IEEE 519-2014 refer to steady-state operation and are indicated to be measured in worst case scenario, at peak demand consumption. The limits are related to the relationship between the short circuit current at the PCC and the load current. The higher the short circuit current, which indicates lower short-circuit impedance and therefore smaller effect of current harmonics on mains network voltage, the higher the limits for harmonics. Those limits are summarized in Tables A.2 and A.3, where TDD refers to Total Demand Distortion, i.e., the ratio of the root mean square of the harmonic content, considering harmonic components up to the 50th order and specifically excluding interharmonics, expressed as a percent of the maximum demand current.

Table A.2: Current Distortion Limits for General Distribution Systems (120 V Through 69 000 V)

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics)						
I_{SC}/I_L	< 11	$11 < h < 17$	$17 < h < 23$	$11 < h < 17$	$35 \leq h$	TDD
$< 20^*$	4.0	2.0	1.5	0.6	0.3	5.0
$20 < 50$	7.0	3.5	2.5	1.0	0.5	8.0
$50 < 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 < 1000$	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

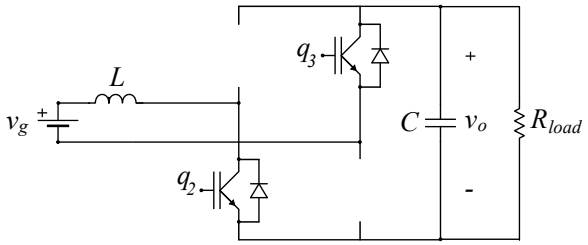
Table A.3: Current Distortion Limits for General Subtransmission Systems (69 001 V Through 161 000 V)

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics)						
I_{SC}/I_L	< 11	$11 < h < 17$	$17 < h < 23$	$23 < h < 35$	$35 \leq h$	TDD
$< 20^*$	2.0	1.0	0.75	0.3	0.15	2.5
$20 < 50$	3.5	1.75	1.25	0.5	0.25	4.0
$50 < 100$	5.0	2.25	2.0	0.75	0.35	6.0
$100 < 1000$	6.0	2.75	2.5	1.0	0.5	7.5
> 1000	7.5	3.5	3.0	1.25	0.7	10.0

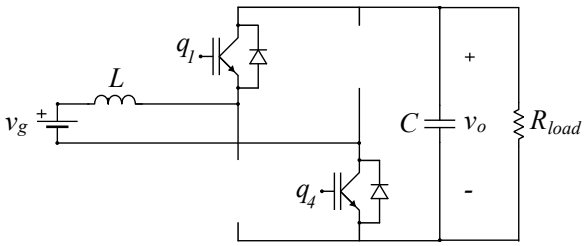
Appendix B

Deduction of the Dynamic Model

The two operation modes are shown in Figure B.1. The state $S1$ corresponds to when switches 2 and are conducting B.1-(a), and the state $S2$ to switches 2 and conducting B.1-(b).



(a) S = 1 - Switches q_2 and q_3 conducting



(b) S =0 - Switches q_1 and q_4 conducting

Figure B.1: Operation Configurations for bipolar PWM operation mode of the Full-Bridge Single-Phase Converter

The first configuration is represented in the state-space as

$$\dot{\mathbf{x}} = \mathbf{A_1}\mathbf{x} + \mathbf{B_1}\mathbf{u} \tag{B.1}$$

with

$$A_1 = \begin{bmatrix} -\frac{r_L}{L} & \frac{1}{L} \\ -\frac{1}{C} & -\frac{1}{R_{DC}C} \end{bmatrix} \tag{B.2}$$

$$B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{B.3}$$

$$\mathbf{x} = \begin{bmatrix} i_g \\ V_o \end{bmatrix} \tag{B.4}$$

$$\mathbf{u} = \begin{bmatrix} v_g \end{bmatrix} \tag{B.5}$$

The second configuration is represented in the state-space as

$$\dot{\mathbf{x}} = \mathbf{A_2}\mathbf{x} + \mathbf{B_2}\mathbf{u} \tag{B.6}$$

with

$$\mathbf{A_2} = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_{DC}C} \end{bmatrix} \tag{B.7}$$

$$\mathbf{B_2} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{B.8}$$

The state space averaged model of the full bridge single phase converter is obtained in the form

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{B.9}$$

with

$$A = dA_1 + (1-d)A_2 = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1-2d}{L} \\ \frac{1-2d}{C} & -\frac{1}{R_{DC}C} \end{bmatrix} \tag{B.10}$$

$$\mathbf{B} = d\mathbf{B_1} + (1-d)\mathbf{B_2} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{B.11}$$

Making the small signal analysis considering

$$\mathbf{x} = \bar{\mathbf{x}} + \hat{\mathbf{x}} \tag{B.12}$$

$$d = \bar{d} + \hat{d} \tag{B.13}$$

Applying to Eq. B.9 It is obtained

$$\dot{\hat{\mathbf{x}}} = \mathbf{A_g}\hat{\mathbf{x}} + \mathbf{B_g}\hat{d} \tag{B.14}$$

with

$$\mathbf{A_g} = \bar{d}\mathbf{A_1} + (1-\bar{d})\mathbf{A_2} \tag{B.15}$$

$$\mathbf{B_g} = (\mathbf{A_1} - \mathbf{A_2})\bar{\mathbf{x}} + (\mathbf{B_1} - \mathbf{B_2})\mathbf{u} \tag{B.16}$$

Applying the Laplace Transform

$$s\mathbf{I}\hat{\mathbf{x}}(s) = \mathbf{A_g}\hat{\mathbf{x}}(s) + \mathbf{B_g}\hat{d}(s) \tag{B.17}$$

Then the transfer function can be put in the form

$$\hat{\mathbf{x}}(s) = [s\mathbf{I} - \mathbf{A_g}]^{-1}\mathbf{B_g}\hat{d}(s) \tag{B.18}$$

Therefore

$$\begin{bmatrix}\hat{I}_g(s)\\ \hat{V}_o(s)\end{bmatrix} = \begin{bmatrix}s+\frac{r_L}{L} & \frac{1-2\bar{d}}{L}\\ -\frac{1-2\bar{d}}{C} & s+\frac{1}{R_{DC}C}\end{bmatrix}^{-1}\begin{bmatrix}\frac{2\bar{V}_o}{L}\\ -\frac{2\bar{I}_L}{C}\end{bmatrix} \tag{B.19}$$

Defining

$$\begin{bmatrix}H_1(s)\\ H_2(s)\end{bmatrix} = \frac{LC}{LCs^2 + \left(\frac{L}{R_{DC}} + Cr_L\right)s + \left(\frac{R_L}{R_{DC}} + (1-2\bar{D})^2\right)}\begin{bmatrix}s+\frac{1}{R_{DC}C} & -\frac{1-2\bar{d}}{L}\\ \frac{1-2\bar{d}}{C} & s+\frac{r_L}{L}\end{bmatrix}\begin{bmatrix}\frac{2\bar{V}_o}{L}\\ -\frac{2\bar{I}_L}{C}\end{bmatrix} \tag{B.20}$$

$H_1(s)$ and $H_2(s)$ are the duty-cycle to line current and Bus voltage, respectively, i.e.

$$H_1(s) = \frac{\hat{I}_g(s)}{\hat{d}(s)} = 2C\bar{V}_o\frac{s+\frac{2}{R_{DC}C}}{LCs^2 + \left(\frac{L}{R_{DC}} + Cr_L\right)s + \left(\frac{R_L}{R_{DC}} + (1-2\bar{d})^2\right)} \tag{B.21}$$

$$H_2(s) = \frac{\hat{V}_o(s)}{\hat{d}(s)} = 2\bar{V}_o\frac{-s\frac{L}{(1-2\bar{d})R_{DC}} - \frac{r_L}{(1-2\bar{d})R_{DC}} + (1-2\bar{d})}{LCs^2 + \left(\frac{L}{R_{DC}} + Cr_L\right)s + \left(\frac{R_L}{R_{DC}} + (1-2\bar{d})^2\right)} \tag{B.22}$$

Considering $r_L \approx 0$

$$\frac{\hat{I}_g(s)}{\hat{d}(s)} = 2C\frac{\bar{V}_o}{(1-2\bar{d})^2}\frac{s+\frac{2}{R_{DC}C}}{\frac{LC}{(1-2\bar{d})^2}s^2 + \frac{L}{(1-2\bar{d})^2R_{DC}}s + 1} \tag{B.23}$$

$$\frac{\hat{V}_o(s)}{\hat{d}(s)} = 2\frac{\bar{V}_o}{(1-2\bar{d})}\frac{1 - s\frac{L}{(1-2\bar{d})^2 R_{DC}}}{\frac{LC}{(1-2\bar{d})^2}s^2 + \frac{L}{(1-2\bar{d})^2 R_{DC}}s + 1} \tag{B.24}$$

Considering

$$V_o = \frac{V_g}{(1-2d)} \tag{B.25}$$

It becomes

$$\frac{\hat{I}_g(s)}{\hat{d}(s)} = 2C\frac{\bar{V}_g}{(1-2\bar{d})^3}\frac{s + \frac{2}{R_{DC}C}}{\frac{LC}{(1-2\bar{d})^2}s^2 + \frac{L}{(1-2\bar{d})^2 R_{DC}}s + 1} \tag{B.26}$$

$$\frac{\hat{V}_o(s)}{\hat{d}(s)} = 2\frac{\bar{V}_g}{(1-2\bar{d})^2}\frac{1 - s\frac{L}{(1-2\bar{d})^2 R_{DC}}}{\frac{LC}{(1-2\bar{d})^2}s^2 + \frac{L}{(1-2\bar{d})^2 R_{DC}}s + 1} \tag{B.27}$$