PROJETO REDE LOCAL CITIBANK

RELATÓRIO TÉCNICO Nº 2

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1 - INTRODUÇÃO

Como parte da especificação de uma rede local para o CITIBANK, são descritos nesse relatório, os objetivos da rede, a arquitetura e método de acesso escolhido para sua implementação e os experimentos de laboratório a serem feitos, visando orientar a escolha do método de codificação da linha, velocidade de transmissão, formato e tamanho máximo do pacote além de servir como uma verificação de viabilidade da solução proposta.

2 - OBJETIVOS

O objetivo da rede local é basicamente conectar microcomputadores e terminais não inteligentes, obedecendo as restrições abaixo:

- Utilizar componentes disponíveis no Brasil; o que se justifica pelas dificuldades existentes para importações de peças nesse setor e pela intenção de prestigiar produtos e tecnologia nacionais;

- Baixo custo; uma vez que a rede deverá conectar basicamente micros, seu custo deve ser compatível com os desses equipamentos;

- Controle inteiramente distribuído; para evitar que uma estação tenha funções de controle e com isso, caso sofra uma pane, provoque a paralisação total da rede;

- Transmissão de dados apenas; não se pretende utilizar a rede para transmitir voz ou imagem;

- Facilidades para manutenção; numa rede com centenas de equipamentos conectados em um prédio, a rápida localização de uma falha só pode ser feita se forem previstos procedimentos que facilitem essa localização e reparo;

- Segurança; devem ser definidos procedimentos e o nível em que a autenticação e a segurança das comunicações será feita.

3 - ARQUITETURA ADOTADA

Levando-se em conta os objetivos e restrições mencionados, optou-se por uma rede com as seguintes características:

Topologia

Barra simples, por permitir controle inteiramente distribuído;

Método de Acesso

CSMA ou CSMA/CD, dependendo de uma avaliação do desempenho do método comparado com a complexidade da implementação;

Meio de Transmissão

Par trançado AWG 22, por ser disponível no Brasil, barato, e permitir fácil adição de novas estações;

Distância Máxima

Aproximadamente 1 Km. Essa limitação deve-se a relação distância máxima x velocidade de transmissão em par trançado. A distância máxima será fixada definitivamente após determinarmos a velocidade de transmissão;

Número Máximo de Estações

255. Esse número foi escolhido de forma arbitrária, levando-se em conta que atende às necessidades iniciais do Banco e limita em 8 (oito) o número de bits necessários para endereçá-las, o que facilita o uso de pastilhas já existentes. Um endereço foi reservado para difusão (broadcast) de mensagens.

4 - PLANEJAMENTO DOS EXPERIMENTOS DE LABORATÓRIO

Visando orientar a especificação e projeto da rede, bem como verificar a viabilidade das soluções propostas e sua compatibilidade com os objetivos, planejou-se fazer em laboratório uma série de experimentos das diversas partes constituintes da rede, de forma hierárquica, como mostrado na figura abaixo.

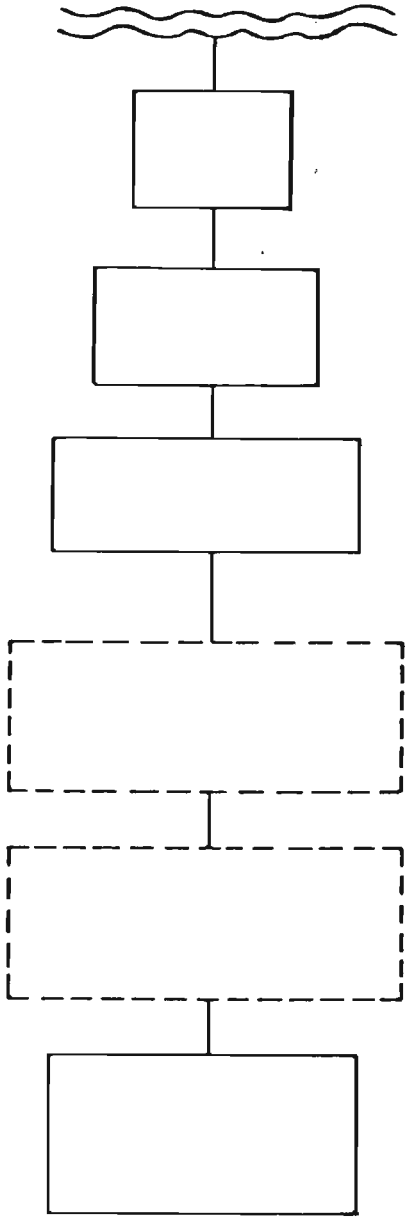

FIGURA 1: PARTES QUE CONSTITUEM A REDE

A seguir são descritos estes experimentos.

4.1 - MEDIÇÃO DAS CARACTERÍSTICAS DO MEIO ESCOLHIDO

O cabo escolhido como meio de comunicação se constitui de par trançado AWG 22, que é facilmente encontrado no mercado nacional por baixo custo.

As principais características do cabo são:

. Proteção exterior de PVC nos dois fios;

. Impedância característica: 100 KHz - 113 Ohms
500 KHz - 104 Ohms
1 MHz - 100 Ohms
5 MHz - 100 Ohms

. Capacitância nominal do cabo: 50 nF/Km

Foi medida a atenuação do cabo em função da frequência (sinal senoidal) para os comprimentos de 100, 200, 500 e 1000 metros. As medidas foram feitas diretamente no fio, isto é, não foram feitas simulações.

Para estas medidas, fez-se o casamento de impedância entre o cabo e o gerador de sinais utilizado, a fim de evitar reflexão de onda e distorcer os resultados obtidos. O esquema utilizado é mostrado na figura 2.

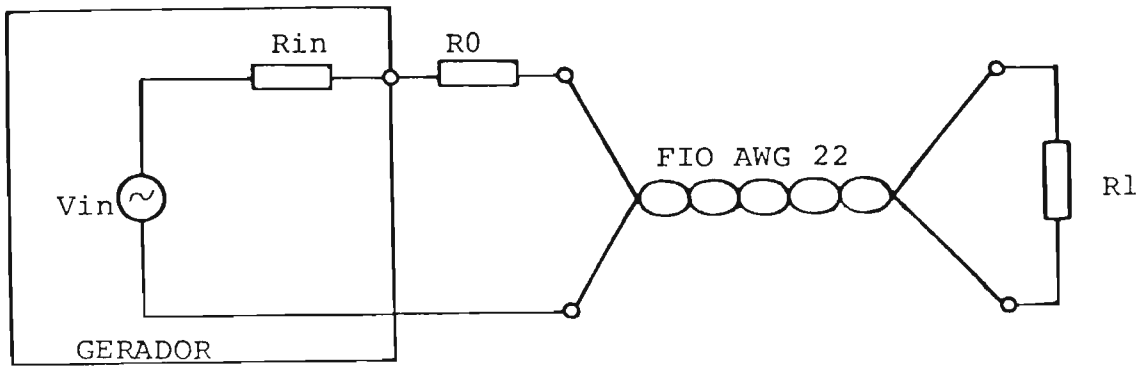

FIGURA 2: ESQUEMA DAS MEDIDAS

A resistência interna do gerador é de 50 Ohms, e considerando-se a curva de impedância do cabo (figura 3), os seguintes valores de R_0 e R_1 foram utilizados:

f < 50 KHz →	medidas não foram feitas	
50 KHz < f < 200 KHz →	$R_0 = 100 + 10 = 110$	
	$R_1 = 56 + 4,7 = 60,7$	
200 KHz < f < 1 MHz →	$R_0 = 100 + 5,6 = 105,6$	
f > 1 MHz →	$R_0 = 100$	
	$R_1 = 47 + 3,3 = 50,3$	

Os resultados são mostrados nas figuras 4 e 5.

4.2 - ACOPLAMENTO DA ESTAÇÃO COM O MEIO DE TRANSMISSÃO

Na barra de comunicação, pretende-se implementar o padrão EIA RS-422 para os sinais elétricos. Esse padrão foi escolhido porque é mais propício para transmissão em alta velocidade, pois trabalha com circuitos balanceados nos quais nenhum dos dois fios é a referência (terra). Foi adotada, então, a utilização de circuitos diferenciais pela sua maior imunidade a ruídos.

Usando-se circuitos diferenciais, o transmissor coloca em cada fio da barra sinais iguais e com sentidos contrários em relação ao seu referencial. O receptor faz a diferença entre estes sinais para obter uma cópia do que foi transmitido. Se algum ruído ocorrer, ele provocará uma perturbação igual nos dois fios pois eles são trançados e quando o receptor fizer a diferença, o ruído será eliminado. Isto pode ser visto na figura 6.

A vantagem na utilização do padrão RS-422 é que ele já se encontra totalmente definido e divulgado, além de existirem circuitos integrados que satisfazem a este padrão. O padrão RS-422 já é utilizado em várias redes locais como por exemplo a OMNINET. Em anexo é apresentada a definição completa do padrão RS-422.

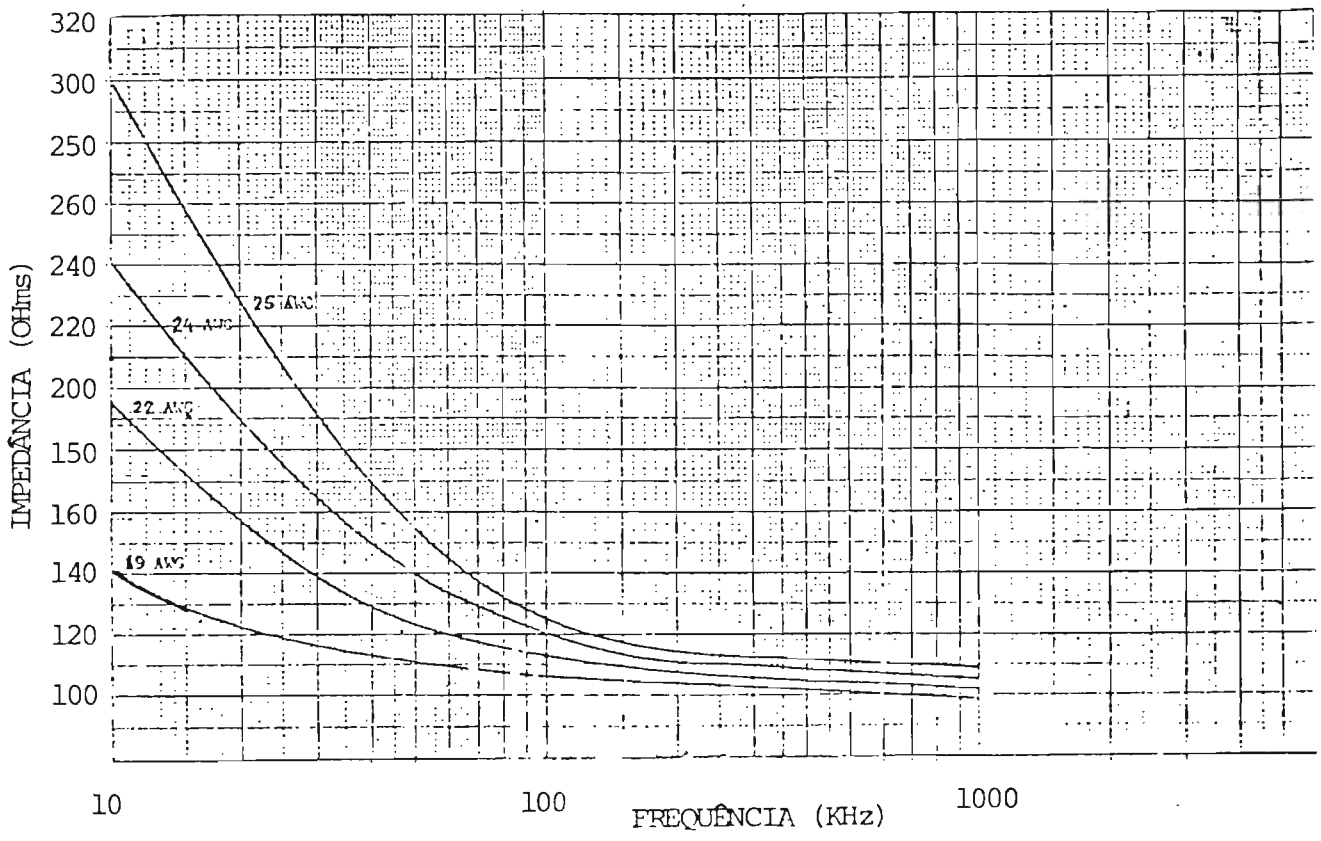

FIGURA 3: CURVA DE IMPEDÂNCIA CARACTERÍSTICA.

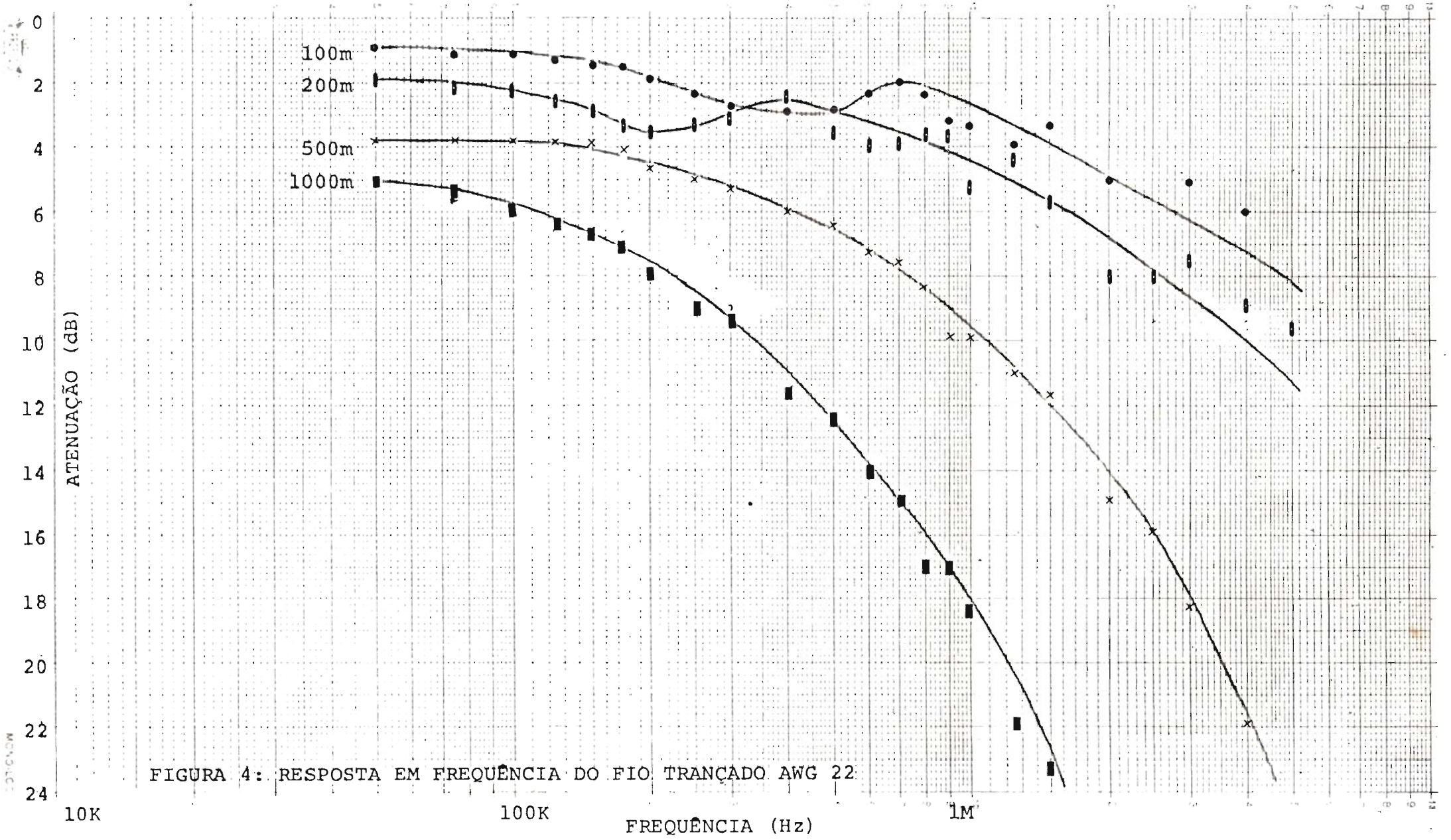

FIGURA 4: RESPOSTA EM FREQUÊNCIA DO FIO TRANÇADO AWG 22

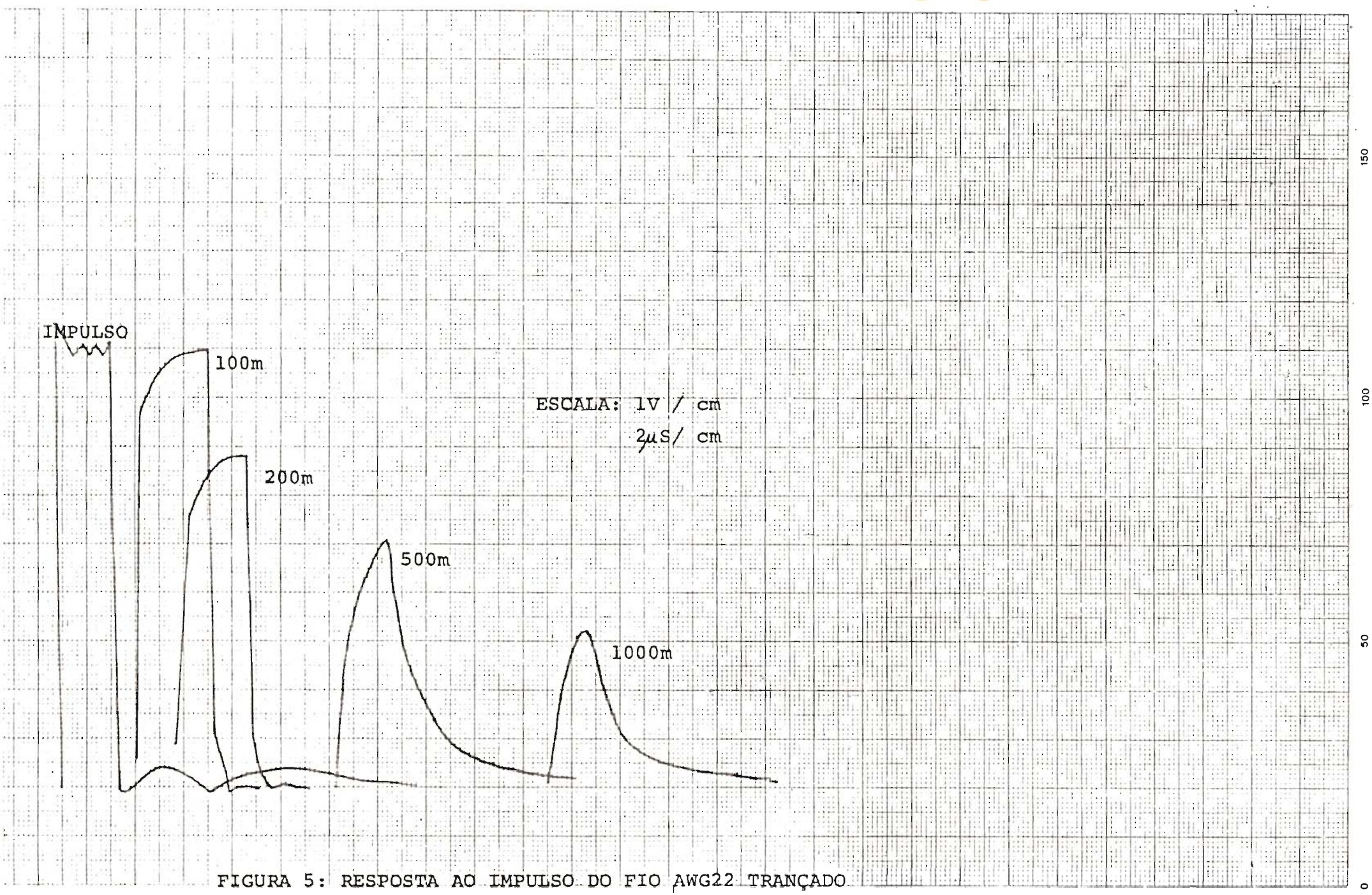

FIGURA 5: RESPOSTA AO IMPULSO DO FIO AWG22 TRANÇADO

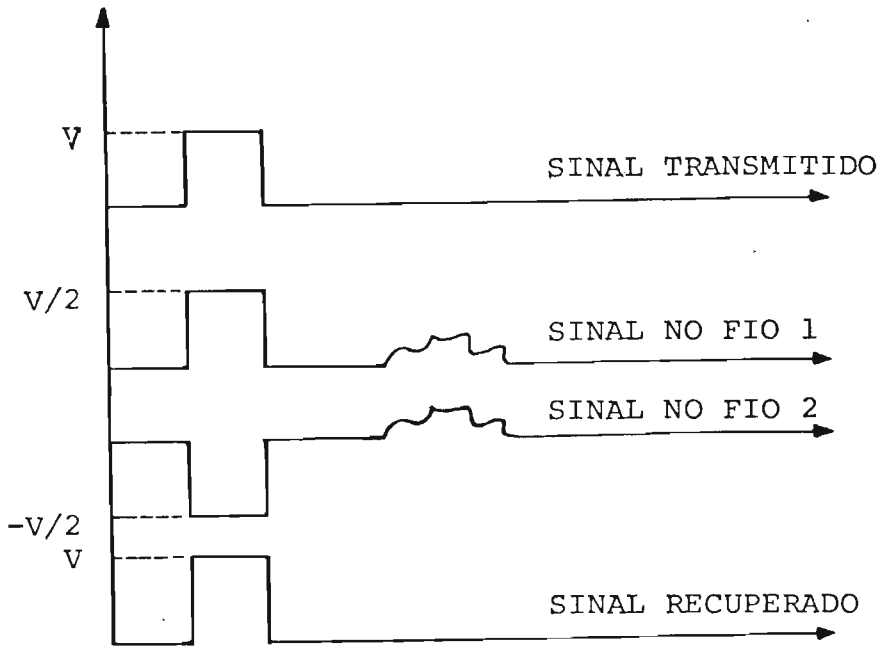

FIGURA 6: UTILIZAÇÃO DE CIRCUITOS DIFERENCIAIS

Uma estação se conecta à barra de comunicação através de um circuito que converte os sinais digitais em elétricos no padrão RS-422, quando a estação está transmitindo, e de outro circuito que converte sinais elétricos no padrão RS-422 para digitais, quando a estação está recebendo. O primeiro circuito é chamado "LINE DRIVER", e o segundo "LINE RECEIVER".

Um fator que pode danificar estes circuitos é a diferença de potencial nas referências dos equipamentos (terra), principalmente em redes maiores, quando se torna difícil ligar todos os equipamentos no mesmo referencial.

Assim é necessário desacoplar as estações da barra de comunicação, o que pode ser feito utilizando-se transformadores de pulso. A estação, então, se conectará à barra como é mostrado na figura 7.

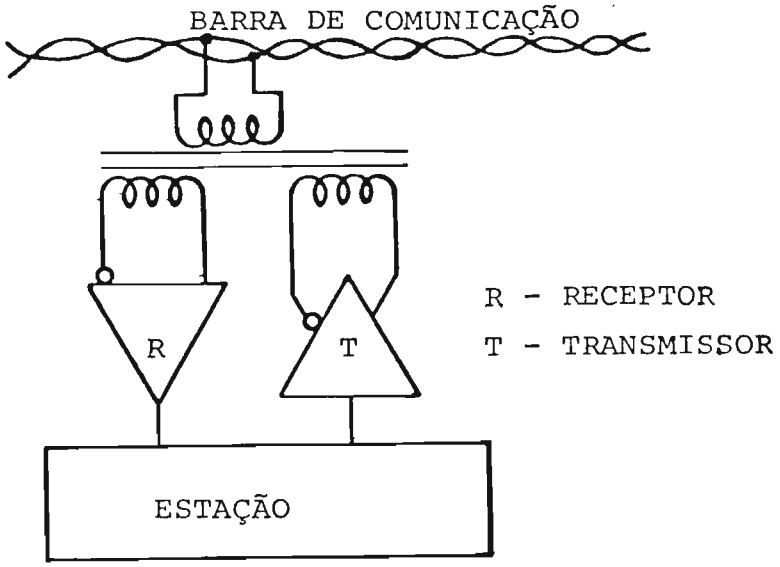

FIGURA 7: CONEXÃO DA ESTAÇÃO À BARRA

De forma a manter o transmissor, o receptor, e a barra obedecendo ao padrão RS-422, os três enrolamentos do transformador de pulso deverão ter o mesmo número de espirais (Relação 1:1).

Para que a configuração da figura 7 seja adequada, o circuito transmissor deve ser capaz de se desconectar da barra quando não estiver ativo, não carregando desnecessariamente a barra, isto é, o circuito transmissor deve ter um estado de alta impedância.

Baseado no que foi dito, os seguintes circuitos integrados podem ser utilizados, considerando-se as suas características dadas abaixo:

a) Transmissor: SN75159 da TEXAS ou similar

- Obedece ao padrão EIA RS-422
- Alimentação única de 5V
- Opera com linha balanceada
- Compatível com TTL e DTL
- Estado de alta impedância na saída para aplicações em linha compartilhada
- Frequência máxima de operação superior a 25 MHz
- Proteção contra curto circuito
- Corrente de saída máxima de 40mA

b) Receptor: SN75157 da TEXAS ou similar

- Obedece ao padrão EIA RS-422
- Alimentação única de 5V
- Tensão de modo comum ± 15V

4.3 - ESTUDO E TESTE COMPARATIVO DE MÉTODOS DE CODIFICAÇÃO

Os métodos de codificação mais usados são mostrados na figura 8 e explicados a seguir.

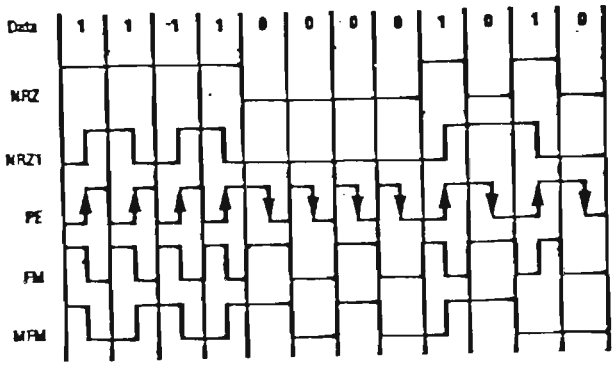

FIGURA 8: MÉTODOS DE CODIFICAÇÃO MAIS USADOS

a) NRZ - "Não Retorno a Zero". Nele, o nível "1" é representado por uma tensão diferente de zero, e o nível "Ø" por uma tensão igual a zero. Esta codificação é deficiente por ser extremamente sensível a transições causadas por ruído, além de não permitir uma auto-sincronização, que consiste em retirar da própria informação um sinal de sincronismo;

b) NRZI - "Não Retorno a Zero Invertido". Foi desenvolvido para aumentar a imunidade a ruído, mas ainda assim possui uma resposta contínua para uma sequência de zeros. Tanto o NRZ como o NRZI possuem a vantagem de necessitarem apenas uma transição por BIT, mas nenhum deles é auto-sincronizável;

c) PE - "Codificação em Fase". Oferece auto-sincronismo que é conseguido garantindo-se que sempre haverá transições , qualquer que seja a sequência de bits. No entanto, ocupa o dobro da banda passante necessária para representar a informação, pois necessita de duas transições por bit. Este método é também chamado de "Codificação Manchester", e é usado na rede "Ethernet" da Xerox;

d) FM - "Modulação em Frequência". É semelhante à codificação PE, no que se refere a auto-sincronização e ao número de transições por bit, porém não requer um controle de mudança de polaridade do sinal;

e) MFM - "Modulação em Frequência Modificada". É um melhoramento sobre o método FM porque utiliza apenas uma transição por bit. Neste método, o nível do sinal é trocado no meio do bit para bits em "1", e no final do bit entre bits consecutivos em "Ø". Este método é usado na rede experimental do projeto REDLAC no Instituto de Matemática na Universidade Nacional Autônoma do México.

Dos métodos apresentados, serão testadas as modulações em fase (PE) e em frequência modificada (MFM). Esses métodos foram escolhidos por serem auto-sincronizáveis, isto é, não neces

sitam de um fio adicional com o sinal de sincronismo, e por já serem usados em outras redes.

Os métodos serão comparados considerando-se a complexidade e custo dos circuitos de modulação/demodulação, o aproveitamento da banda passante, e o uso efetivo do canal. Este último, consiste em se saber a sequência de bits que deve anteceder à mensagem a ser transmitida, de forma a se garantir que o transmissor e os receptores ligados à barra sincronizem os seus sinais de temporização ("clock").

4.4 - PROJETO E TESTE DO MECANISMO DE DETEÇÃO DE COLISÃO

Um método simples de transmissão, chamado ALOHA, consiste em não fazer nenhuma verificação na barra para começar a transmissão. Se uma transmissão já estiver sendo executada simultaneamente por outra estação ocorre uma colisão, e os sinais da barra não corresponderão ao que foi transmitido. Neste caso a colisão só será detectada pelo receptor no final da mensagem, quando este computar os bits de verificação da mensagem ("checksum"). Deve ser observado que o transmissor não toma conhecimento da colisão.

Outro método, chamado de "Carrier-Sense Multiple-Access" (CSMA), consiste em se verificar se alguma transmissão está sendo executada, e só começar a transmissão quando não houver sinais na barra, isto é, não houver transmissões ativas. Quando a transmissão se inicia, nenhuma verificação é efetuada na barra. Colisões podem ocorrer se mais de uma estação estiver esperando que a transmissão em execução termine para começar a transmitir, recaindo, então, no caso anterior.

Um método mais eficiente, chamado "Carrier-Sense Multiple-Access with Collision-Detection" (CSMA-CD), consiste

em se monitorar o sinal que se está transmitindo durante a transmissão, em adição ao que é feito no método CSMA. Quando se verificar uma diferença entre o bit recebido pela própria estação transmissora e o bit que se deseja transmitir, a transmissão continua durante um tempo suficiente para que todas as estações que estejam transmitindo detectem a colisão, e a transmissão é encerrada. Nova tentativa de transmissão é feita algum tempo depois, tempo esse que é diferente para cada estação.

O método com deteção de colisão tem três vantagens:

. A estação sabe, quando uma colisão é detectada, que sua mensagem foi transmitida com erro, e uma retransmissão pode ser feita imediatamente;

. Mensagens interferidas não são transmitidas até o final, diminuindo o tempo em que a barra fica ocupada por mensagens não aproveitadas, aumentando a eficiência da rede;

. A frequência com que se detecta as colisões pode ser usada para se estimar o tráfego da rede, e para ajustar os intervalos de retransmissão.

Um experimento será feito visando definir qual método será usado, CSMA ou CSMA/CD.

O circuito de deteção de colisão será projetado, de forma que se possa avaliar a sua complexidade e operacionalidade, visando determinar se o método será implementado.

A deteção de colisão é feita monitorando-se a barra durante a transmissão. A nível elétrico, a colisão provoca perturbações no sinal da barra. Se estações muito distantes estão transmitindo ao mesmo tempo, a interferência do sinal transmitido por uma delas pode ter pouca influência no sinal transmitido pela outra.

Esta interferência é função da frequência de transmissão e da distância entre as estações que estão transmitindo, já que quanto maior esses fatores menor é a intensidade do sinal.

As experiências que serão feitas visarão o projeto de circuitos compatíveis com a velocidade de transmissão e o comprimento máximo da rede.

5 - REFERÊNCIAS

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6 - ANEXOS

6.1 - DEFINIÇÃO DO PADRÃO EIA - RS 422

EIA STANDARD

Electrical Characteristics of Balanced Voltage Digital Interface Circuits

RS-422

811

APRIL 1975

Engineering Department

ELECTRONIC INDUSTRIES ASSOCIATION

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ELECTRICAL CHARACTERISTICS OF

BALANCED VOLTAGE DIGITAL INTERFACE CIRCUITS

(From EIA Standards Proposal No. 1162-A, formulated under the cognizance of EIA Committee TR-30.1 on Signal Quality)

1. SCOPE

This standard specifies the electrical characteristics of the balanced voltage digital interface circuit normally implemented in integrated circuit technology that may be employed when specified for the interchange of serial binary signals between Data Terminal Equipment (DTE) and Data Communications Equipment (DCE) or in any interconnection of binary signals between voice or data equipment.

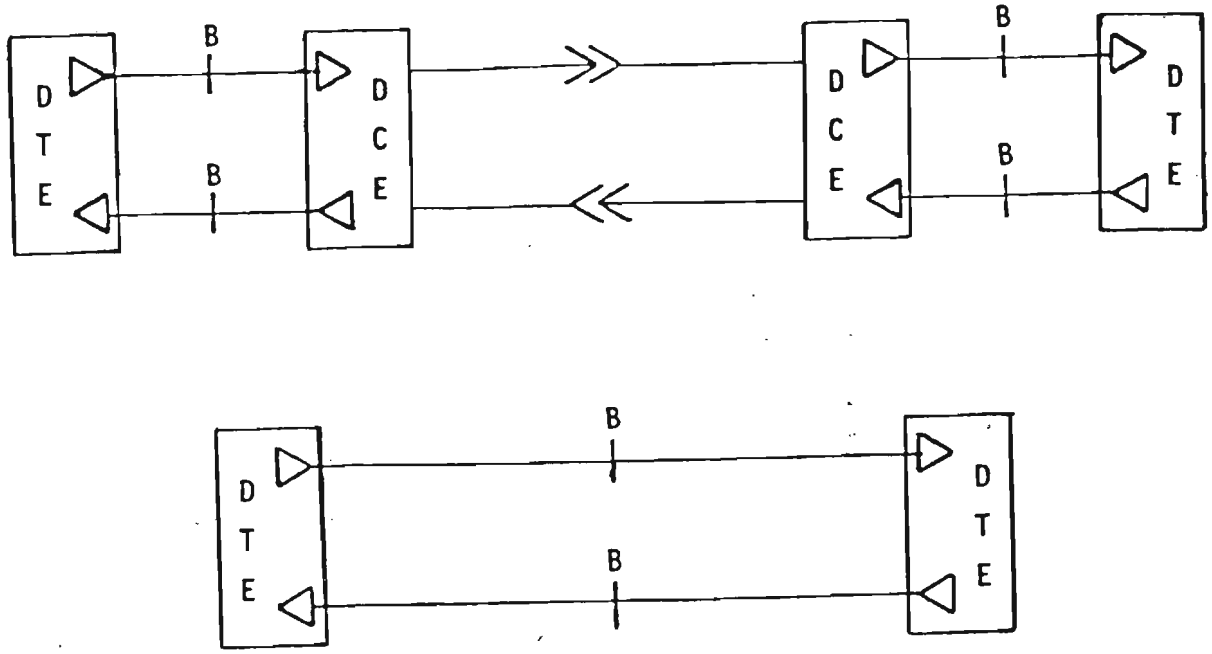
The interface circuit includes a generator connected by a balanced interconnecting cable to a load consisting of a receiver or receivers and an optional termination resistor. The electrical characteristics of the circuit are specified in terms of required voltage, current, and resistance values obtained from direct measurement of the generator and receiver components. The receiver specification for the interface is electrically identical to that specified for the unbalanced interface circuit in RS-423. The characteristics of the interconnecting cable are specified, and guidance is given with respect to limitations on data modulation rate imposed by the parameters of cable length, balance and termination.

The parameter values specified for the balanced generator and load components of the interface are designed such that balanced interface circuits may be used within the same interconnection as unbalanced interface circuits specified by RS-423. For example, the balanced circuits may be used for data and timing while the unbalanced circuits may be used for low speed control functions.

It is intended that this standard will be referenced by other standards that specify the complete DTE/DCE interface (i.e. protocol, timing, pin assignments, etc.) for applications where the electrical characteristics of a balanced voltage digital circuit are required. Applications are also forseen in other areas using binary signal interchange. This standard does not specify other characteristics of the DTE/DCE interface (such as signal quality and timing, etc.) essential for the interconnected equipment operation.

2. CROSS REFERENCE

This standard is one of a series relating to the interconnection of DTE and DCE. Other EIA standards in this series, in addition to RS-423, pertaining to the DTE/DCE and DTE/DTE interface specifications are in existence or in various stages of preparation at the time of publication of this standard. The user is referred to EIA Engineering Headquarters for information on specific standards available.



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Legend:

DTE = Data Terminal Equipment

DCE = Data Communications Equipment

= Interface Generator

= Interface Load

B = Balance Interface Circuit

= Telecommunications Channel

FIGURE 3.1

Applications of Balanced Voltage Digital Interface Circuit

3. APPLICABILITY

The provisions of this standard may be applied to the circuits employed at the interface between equipments where the information being conveyed is in the form of binary signals at the dc base-band level. This standard shall be referenced by the specifications and specific interface standards applying these electrical characteristics. Typical points of applicability for this standard are depicted in Figure 3.1.

The balanced voltage digital interface circuit will normally be utilized on data, timing or control where the modulation rate on these circuits is up to 10 megabauds. Balanced voltage digital interface devices meeting the electrical characteristics of this standard need not operate over the entire modulation rate range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower modulation rates.

While the balanced interface is intended for use at the higher modulation rates, it may, in preference to the unbalanced interface circuit, generally be required where any of the following conditions prevail:

a. The interconnecting cable is too long for effective unbalanced operation.

b. The interconnecting cable is exposed to extraneous noise sources that may cause an unwanted voltage in excess of plus or minus one volt measured differentially between the signal conductor and circuit common at the load end of the cable with a 50 ohm resistor substituted for the generator.

c. It is necessary to minimize interference with other signals.

d. Inversion of signals may be required, e.g., plus MARK to minus MARK may be obtained by inverting the cable pair.

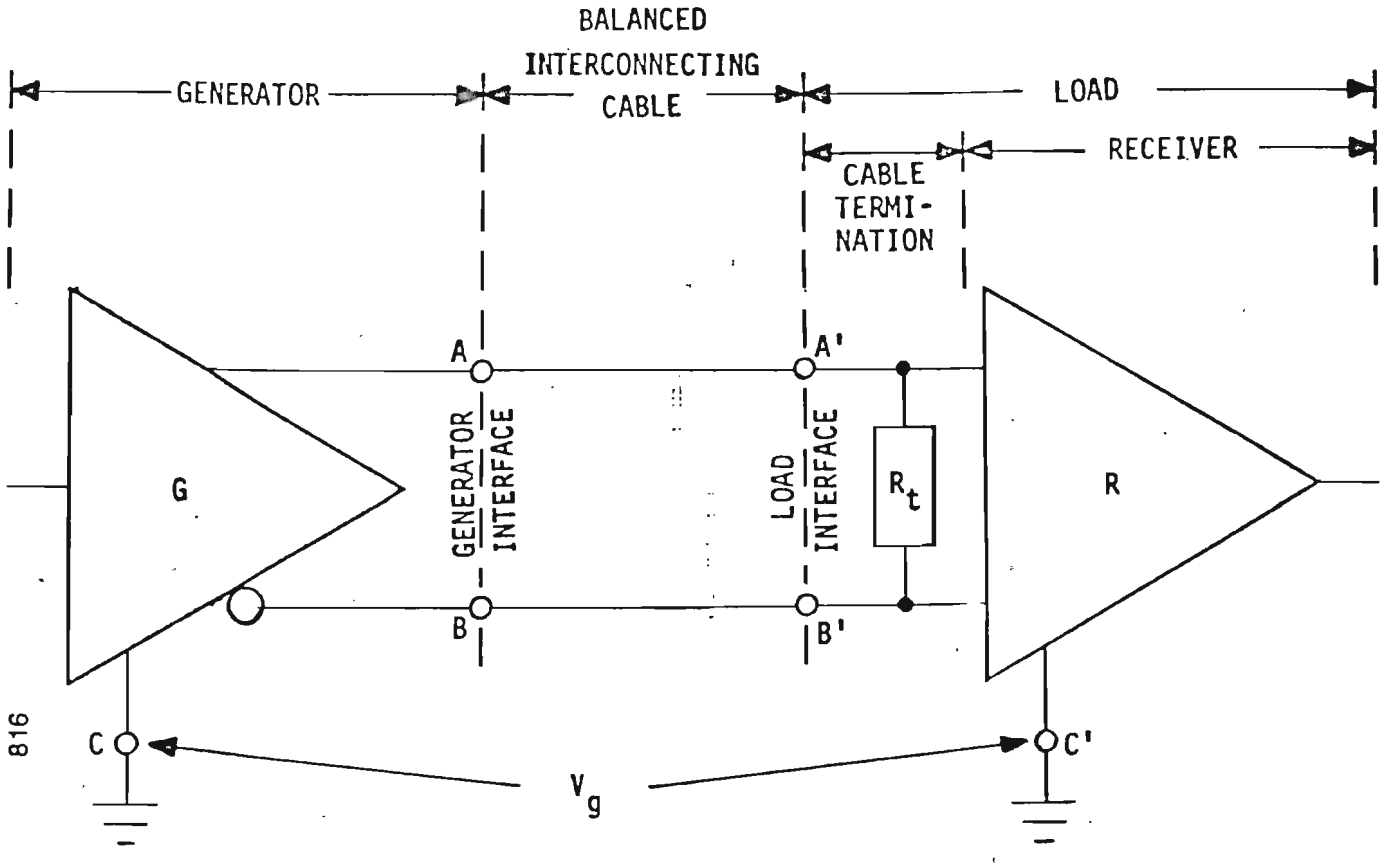
While a restriction on maximum cable length is not specified, guidelines are given with respect to conservative operating distances as a function of modulation rate (see Section 7). In general, these conservative values may be greatly exceeded where the installation is engineered to ensure that noise and ground potential values are held within specified limits.

4. ELECTRICAL CHARACTERISTICS

The balanced voltage digital interface circuit is shown in Figure 4.1. The circuit consists of three parts: the generator, the balanced interconnecting cable, and the load. The load is comprised of one or more receivers (R) and an optional cable termination resistance (R_t). The electrical characteristics of the generator and receiver are specified in terms of direct electrical measurements while the interconnecting cable is specified in terms of its electrical and physical characteristics.

4.1 Generator Characteristics

The generator electrical characteristics are specified in accordance with measurements illustrated in Figures 4.2 and 4.3 and described in paragraphs 4.1.1 through 4.1.5. A generator circuit meeting these requirements results in a low impedance (100 ohms or less) balanced voltage source that will



Legend:

R_t	=	Optional Cable Termination Resistance
V_g	=	Ground Potential Difference
A,B	=	Generator Interface Points
A', B'	=	Load Interface Points
C	=	Generator Circuit Ground
C'	=	Load Circuit Ground

FIGURE 4.1

Balanced Digital Interface Circuit

produce a differential voltage applied to the interconnecting cable in the range of 2 volts to 6 volts. The signalling sense of the voltages appearing across the interconnection cable are defined as follows:

(1) The A terminal of the generator shall be negative with respect to the B terminal for a binary 1 (MARK or OFF) state.

(2) The A terminal of the generator shall be positive with respect to the B terminal for a binary 0 (SPACE or ON) state.

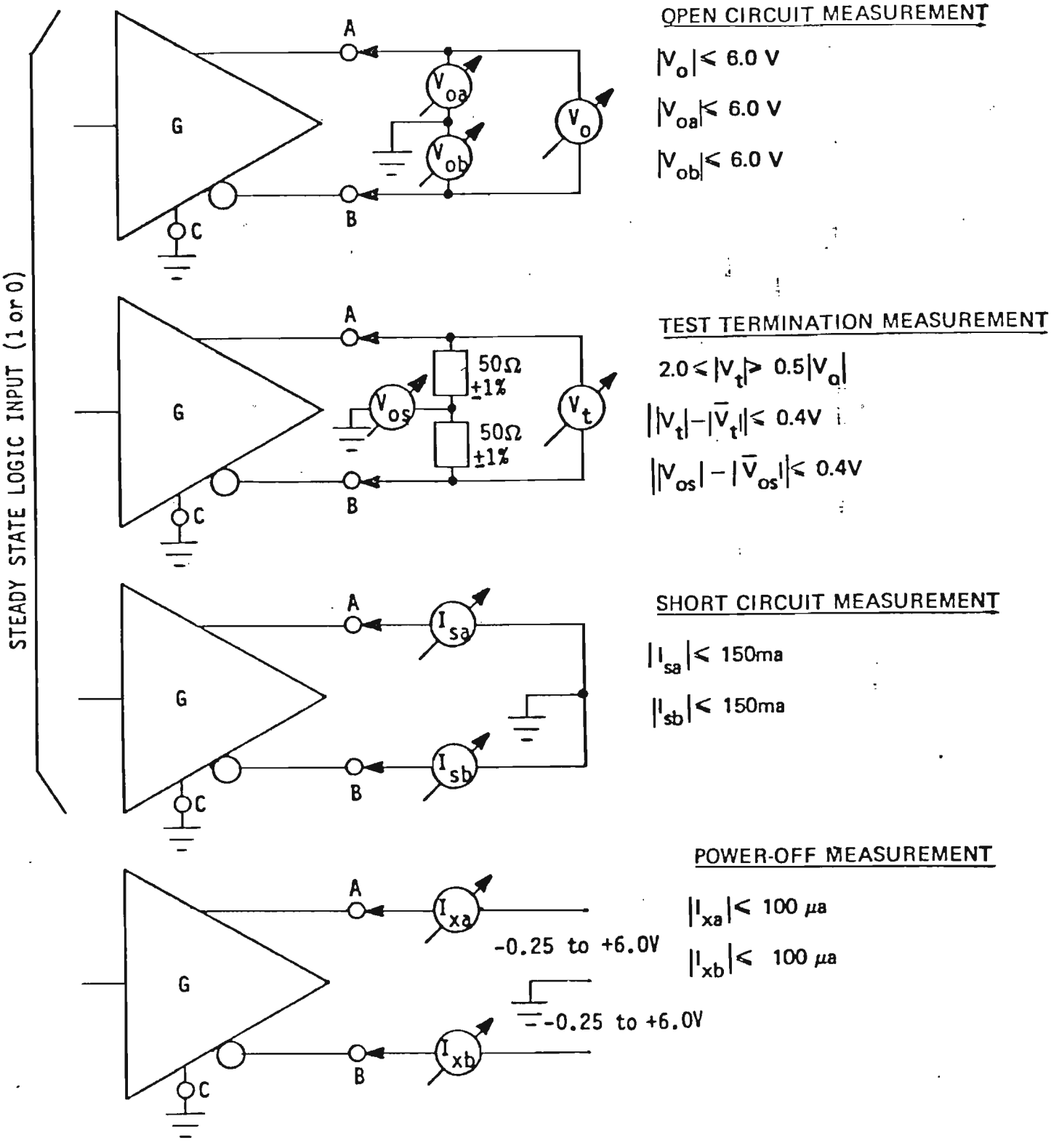
4.1.1 Open Circuit Measurement (Figure 4.2) For either binary state, the magnitude of the differential voltage (Vo) measured between the two generator output terminals shall not be more than 6.0 volts; nor shall the magnitude of Voa and Vob measured between the two generator output terminals and generator circuit ground be more than 6.0 volts.

4.1.2 Test Termination Measurement (Figure 4.2) With a test load of two resistors, 50 ohm ± 1% each, connected in series between the generator output terminals, the magnitude of the differential voltage (V_t) measured between the two output terminals shall not be less than either 2.0 volts or 50% of the magnitude of Vo whichever is greater. For the opposite binary state the polarity of Vt shall be reversed ($\overline{V}t$). The magnitude of the difference in the magnitude of Vt and $\overline{V}t$ shall be less than 0.4 volts. The magnitude of the generator offset voltage Vos measured between the center point of the test load and generator circuit ground shall not be greater than 3.0 volts. The magnitude of the difference in the magnitudes of Vos for one binary state and $\overline{V}os$ for the opposite binary state shall be less than 0.4 volts.

4.1.3 Short-Circuit Measurement (Figure 4.2) With the generator output terminals short-circuited to generator circuit ground, the magnitudes of the currents flowing through each generator output terminal shall not exceed 150 milliamperes for either binary state.

4.1.4 Power-off Measurement (Figure 4.2) Under power-off conditions, the magnitude of the generator output leakage currents (Ixa and Ixb), with voltages ranging between +6.0 and −0.25 volts applied between each output terminal and generator circuit ground, shall not exceed 100 microamperes.

4.1.5 Output Signal Wave Form (Figure 4.3) During transitions of the generator output between alternating binary states (one–zero–one–zero, etc.), the differential signal measured across a 100 ohm ± 10% test load connected between the generator output terminals shall be such that the voltage monotonically changes between 0.1 and 0.9 of Vss within 0.1 of the unit interval or 20 nanoseconds, whichever is greater. Thereafter, the signal voltage shall not vary more than 10% of Vss from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of Vt or $\overline{V}t$ exceed 6 volts, nor be less than 2 volts. Vss is defined as the voltage difference between the two steady state values of the generator output.



OPEN CIRCUIT MEASUREMENT

$|V_o| \leq 6.0$ V

$|V_{oa}| \leq 6.0$ V

$|V_{ob}| \leq 6.0$ V

TEST TERMINATION MEASUREMENT

$2.0 \leq |V_t| \geq 0.5|V_o|$

$||V_t| - |\bar{V}_t|| \leq 0.4$V

$||V_{os}| - |\bar{V}_{os}|| \leq 0.4$V

SHORT CIRCUIT MEASUREMENT

$|I_{sa}| \leq 150$ma

$|I_{sb}| \leq 150$ma

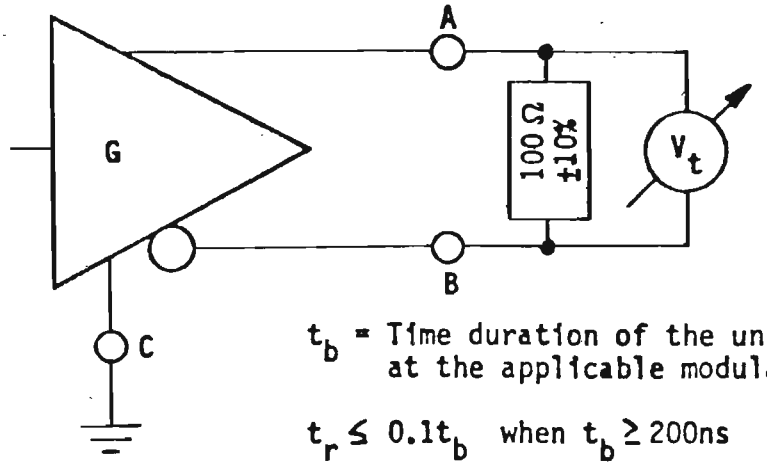
POWER-OFF MEASUREMENT

$|I_{xa}| \leq 100\ \mu$a

$|I_{xb}| \leq 100\ \mu$a

FIGURE 4.2

Generator Parameter Measurements



t_b = Time duration of the unit interval at the applicable modulation rate

$t_r \leq 0.1t_b$ when $t_b \geq 200ns$

$t_r \leq 20ns$ when $t_b < 200ns$

V_{ss} = Difference in steady state voltages

$V_{ss} = |V_t - \overline{V}_t|$

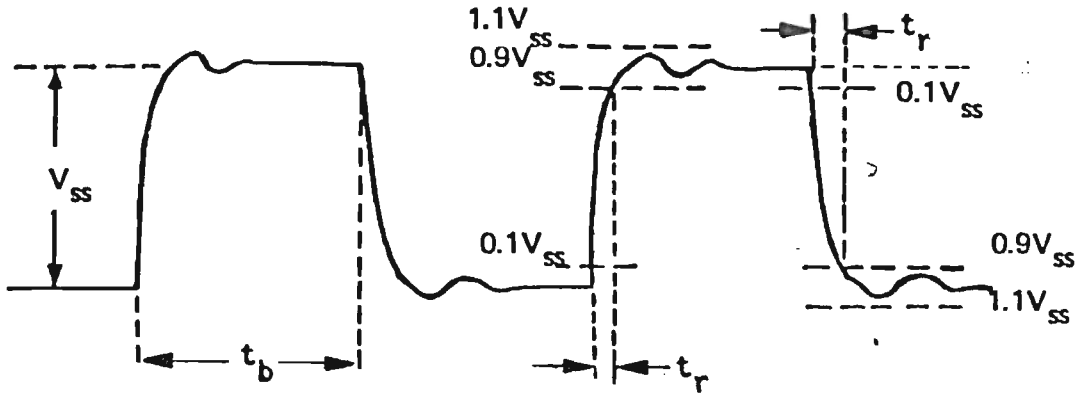


FIGURE 4.3

Generator Output Signal Wave Form

4.2 Load Characteristics

The load consists of a receiver (R) and an optional cable termination resistance (Rt) as shown in Figure 4.1. The electrical characteristics of a single receiver without optional cable termination and fail safe provision are specified in terms of the measurements illustrated in Figures 4.4 through 4.6 and described in paragraphs 4.2.1 through 4.2.5. A circuit meeting these requirements results in a differential receiver having a high input impedance ($\geq$ 4 kohms), a small input threshold transition region between −0.2 and +0.2 volts, and allowance for an internal bias voltage not to exceed 3 volts in magnitude. Multiple receivers and a provision for fail safe operation for specific applications are allowed in the load within the limitations specified in paragraph 4.2.7. The receiver used in the load for the balanced circuit is electrically identical to that specified for the unbalanced interface circuit in RS-423.

4.2.1 Input Current-Voltage Measurements (Figure 4.4) With the voltage Via (or Vib) ranging between −10 and +10 volts, while Vib (or Via) is held at 0 volts (grounded), the resultant input current Iia (or Iib) shall remain within the shaded region shown in the graph in Figure 4.4. These measurements apply with the power supply(s) in both the power-on and power-off conditions.

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4.2.2 Input Sensitivity Measurement (Figure 4.5) Over an entire common mode voltage (Vcm) range of −7 to +7 volts, the receiver shall not require a differential input voltage of more than 200 millivolts to correctly assume the intended binary state. The common mode voltage (Vcm) is defined as the algebraic mean of the two voltages appearing at the receiver input terminals (A′ and B′) with respect to the receiver circuit ground (C′). Reversing the polarity of Vi shall cause the receiver to assume the opposite binary state. The receiver is required to maintain correct operation for differential input signal voltages ranging between 200 millivolts and 6 volts in magnitude. The maximum voltage (signal plus common mode) present between either receiver input terminal and receiver circuit ground shall not exceed 10 volts in magnitude nor cause the receiver to operationally fail. Additionally, the receiver shall tolerate a maximum differential signal of 12 volts applied across its input terminals without being damaged. (NOTE: Designers of terminating hardware should be aware that slow signal transitions with noise present may give rise to instability or oscillatory conditions in the receiving device, and therefore appropriate techniques should be implemented to prevent such behavior. For example, adequate hysteresis may be incorporated into the receiver to prevent such conditions.)

*4.2.3 Input BalanceMeasurement (Figure 4.6)*The balance of the receiver input voltage-current characteristics and bias voltages shall be such that the receiver will remain in the intended binary state when a differential voltage (Vi) of 400 millivolts is applied through 500 ohms ± 1% to each input terminal, as shown in Figure 4.6, and Vcm is varied between −7 and +7 volts. When the polarity of Vi is reversed, the opposite binary state shall be maintained under the same conditions.

FIGURE 4.6 Receiver Input Balance Measurement

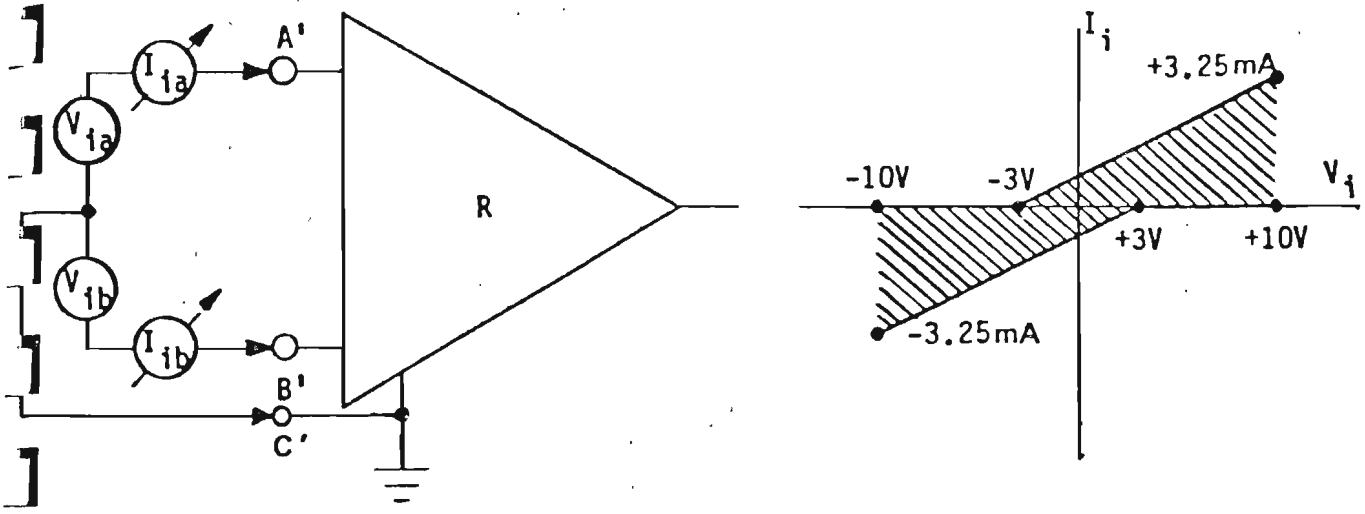


FIGURE 4.4 Receiver Input Current-Voltage Measurement

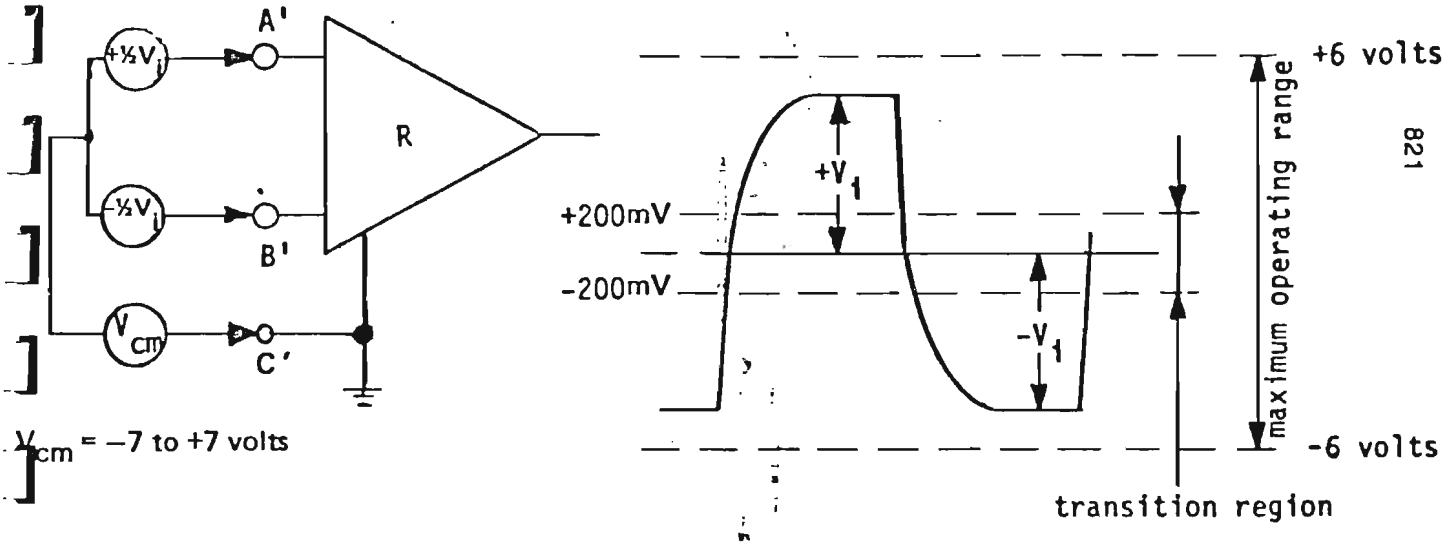
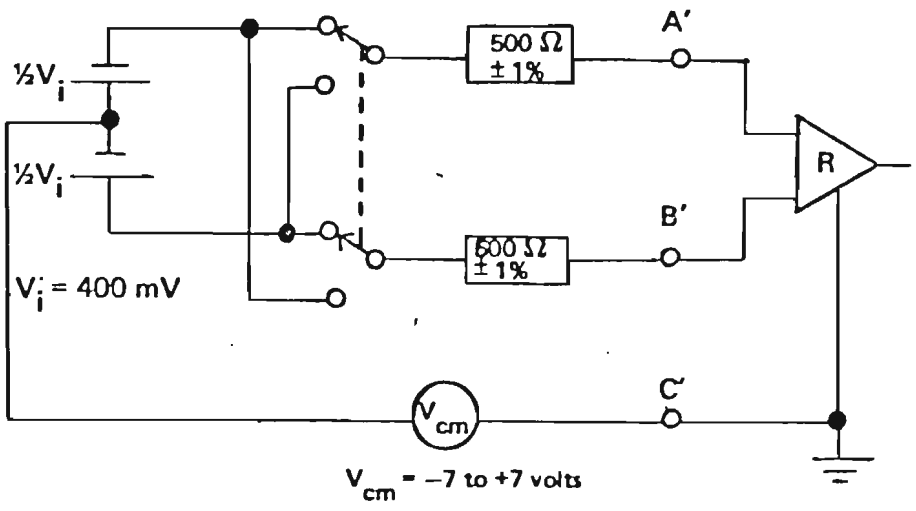


FIGURE 4.5 Receiver Input Sensitivity Measurement



4.2.4 Cable Termination The use of a cable termination (Rt) is optional depending upon the specific environment in which the interface circuit is employed. See paragraph 4.2.7 for limit on total load resistance.

4.2.5 Multiple Receivers The use of up to 10 receivers in the load may be optionally employed. However, extreme caution must be exercised to avoid performance degradation due to signal reflective effects from stub lines emanating from the load interface point to the receivers. See paragraph 4.2.7 for limits on total load resistance and sensitivity.

4.2.6 Fail Safe Operation (Figure 4.7) Other standards and specifications using the electrical characteristics of the balanced voltage digital interface circuit may require that specific interchange leads be made fail safe to certain fault conditions. Where fail safe operation is required by such referencing standards and specifications, a provision shall be incorporated in the load to provide a steady binary condition (either MARK or SPACE as required by the application) to protect against certain fault conditions.

The method of providing fail safe is not standardized, however, the circuit shown in Figure 4.7 will provide a steady binary condition of the receiver for the following fault condition:

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a. Generator power off.

b. Both signal wires open (Signal common return still connected).

c. Generator not implemented (Signal leads may or may not be present).

d. Open connector (Both signal leads and the common signal return are open simultaneously).

The fail safe circuit in Figure 4.7 uses two resistors and a voltage source as shown to produce a steady bias on the receiver in the event of any of the faults a. through d. listed above. In normal operation, the low source resistance of the generator will cause the effect of the bias to become negligible on the receiver slicing level. This circuit will not protect against short circuits across the cable pair, nor will it protect against single open ground returns, and is not applicable where a termination resistance (Rt) is used. (See Section 4.2.7)

If the fail safe is implemented by other methods, additional fault conditions may be detected. For example, a threshold region detector (a window detector to respond when the input signal lies within the −200 to +200 millivolt transition region) in conjunction with a monostable timing device to determine when such a condition (input signal within the transition region) has existed for an abnormal amount of time, will expand fault coverage to include a shorted cable pair (in addition to detecting faults a. through d.) and could be used when the cable termination resistance is present. (For limits on total load characteristics see Section 4.2.7.)

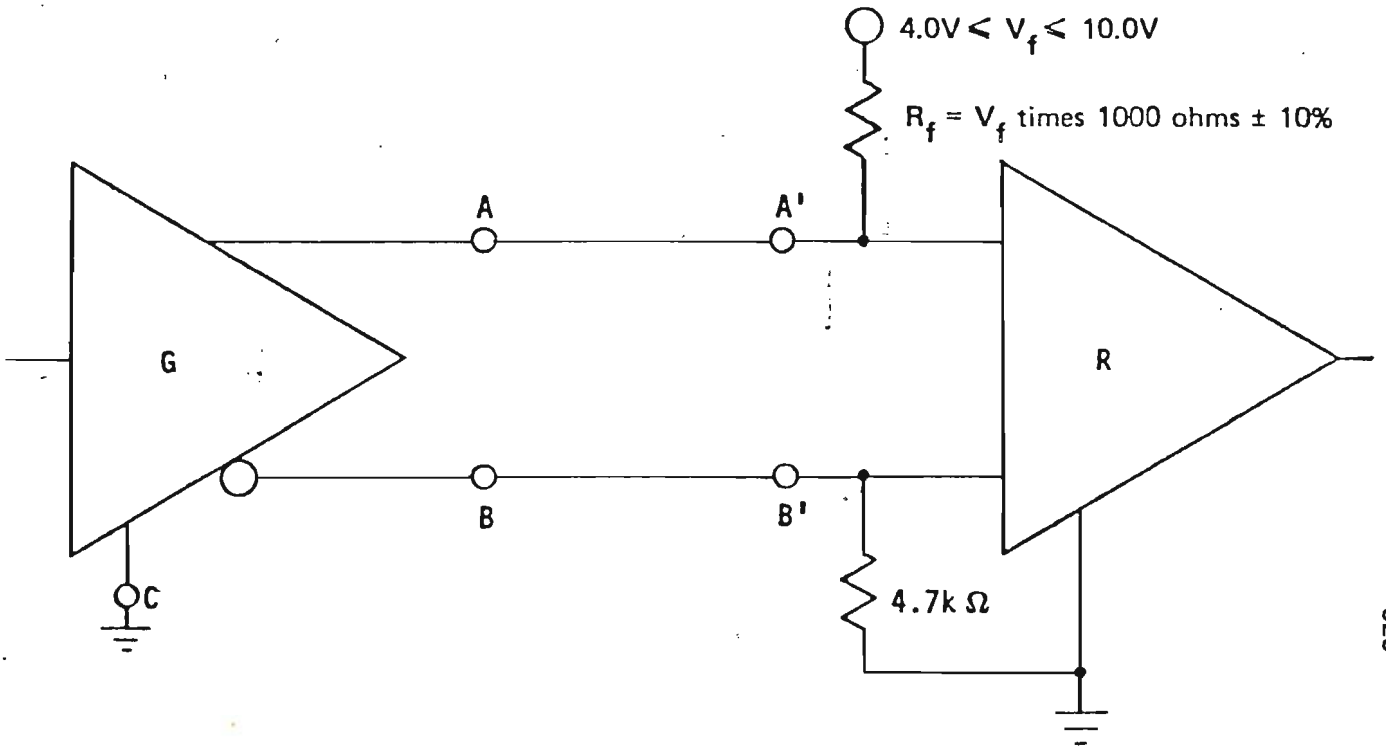

FIGURE 4.7

Example Method of Fail Safe

4.2.7 Total Load Characteristic Limits The total load including multiple receivers, fail safe provision, and cable termination shall have a resistance greater than 90 ohms between its input points (A' and B', Figure 4.1) and shall not require a differential input voltage of more than 200 millivolts for all receivers to assume the intended binary state.

4.3 Interconnecting Cable Characteristics

The characteristics of the interconnecting cable are specified in paragraphs 4.3.1 through 4.3.4, and additional guidance concerning cable characteristics that are not specified is given in Section 7 of this standard. An interconnecting cable meeting these specifications will result in a transmission line with a nominal characteristic impedance on the order of 100 ohms to frequencies greater than 100 kilohertz, and a dc series loop resistance not exceeding 240 ohms. The cable may be composed of twisted or untwisted pair (flat cable) possessing the characteristics described in paragraphs 4.3.1 through 4.3.4 uniformly over its length. Most commonly available cable used for telephone applications should meet these specifications.

4.3.1 Conductor Size The interconnecting cable shall be composed of two wires of a 24 AWG or larger conductor for solid or stranded copper wires, or for non-copper conductors, a sufficient size to yield a dc wire resistance not to exceed 30 ohms per 1000 feet per conductor.

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4.3.2 Mutual Pair Capacitance The capacitance between one wire in the pair to the other wire shall not exceed 20 picofarads per foot, and the value shall be reasonably uniform over the length of the cable.

4.3.3 Stray Capacitance The capacitance between one wire in the cable to all others in the cable sheath, with all others connected to ground, shall not exceed 40 picofarads per foot and shall be reasonably uniform for a given conductor over the length of the cable.

4.3.4 Pair-to-Pair Balanced Crosstalk The balanced crosstalk from one pair of wires to any other pair in the same cable sheath shall have a minimum value of 40 decibels of attenuation measured at 150 kilohertz.

5. ENVIRONMENTAL CONSTRAINTS

A balanced voltage digital interface circuit conforming to this standard will perform satisfactorily at data modulation rates up to 10 megabauds providing that the following operational constraints are simultaneously satisfied·

a. The interconnecting cable length is within that recommended for the applicable modulation rate indicated in Section 7, and the cable is appropriately terminated.

b. The common mode voltage at the receiver is less than 7 volts (peak). The common mode voltage is defined to be any uncompensated combination of generator-receiver ground potential difference, the generator offset voltage (Vos), and longitudinally coupled peak random noise voltage measured between the receiver circuit ground and cable with the generator ends of the cable short-circuited to ground.

6. CIRCUIT PROTECTION

Balanced voltage digital interface generator and receiver devices, under either the power-on or power-off condition, complying with this standard shall not be damaged under the following conditions:

a. Generator open circuit.

b. Short-circuit across the balanced interconnecting cable.

c. Short-circuit to any other lead using electrical characteristics complying with this standard and RS-423.

d. Short circuit to ground.

The above faults b. through d. may cause the power dissipation in the interface devices to approach the maximum power dissipation that may be tolerated by a typical integrated circuit (IC) package. The user is therefore cautioned that where multiple generators or receivers are implemented in a single IC package, only one such fault per package may be tolerated at one time without damage occuring.

The user is also cautioned that the generator and receiver devices complying with this standard may be damaged by spurious voltages applied between their input/output terminals and their circuit grounds. In those applications where the interconnecting cable may be inadvertently connected to other circuits or where it may be exposed to a severe electromagnetic environment, protection should be employed as may be specified in a standard yet to be written.

7. GUIDELINES

When interconnecting equipment using the electrical interface characteristics specified in this standard, certain consideration should be given to some of the problems that may be encountered due to the interconnecting cable characteristics, cable termination resistance, optional grounding arrangements, and interconnection with interfaces using other electrical characteristics.

7.1 Interconnecting Cable

The electrical characteristics of the interconnecting cable are specified in Section 4.3 in this standard. The following section is additional guidance concerning operational constraints imposed by the cable parameters of length and termination resistance.

7.1.1 Length The maximum permissible length of cable separating the generator and load is a function of modulation rate and is influenced by the tolerable signal distortion, the amount of longitudinally coupled noise and ground potential difference introduced between the generator and load circuit grounds as well as by cable balance. Increasing the physical separation and interconnecting cable length between the generator and load interface points, increases exposure to common mode noise, signal distortion, and the effects of cable imbalance. Accordingly, users are advised to restrict cable length to a minimum, consistent with the generator-load physical separation requirements.

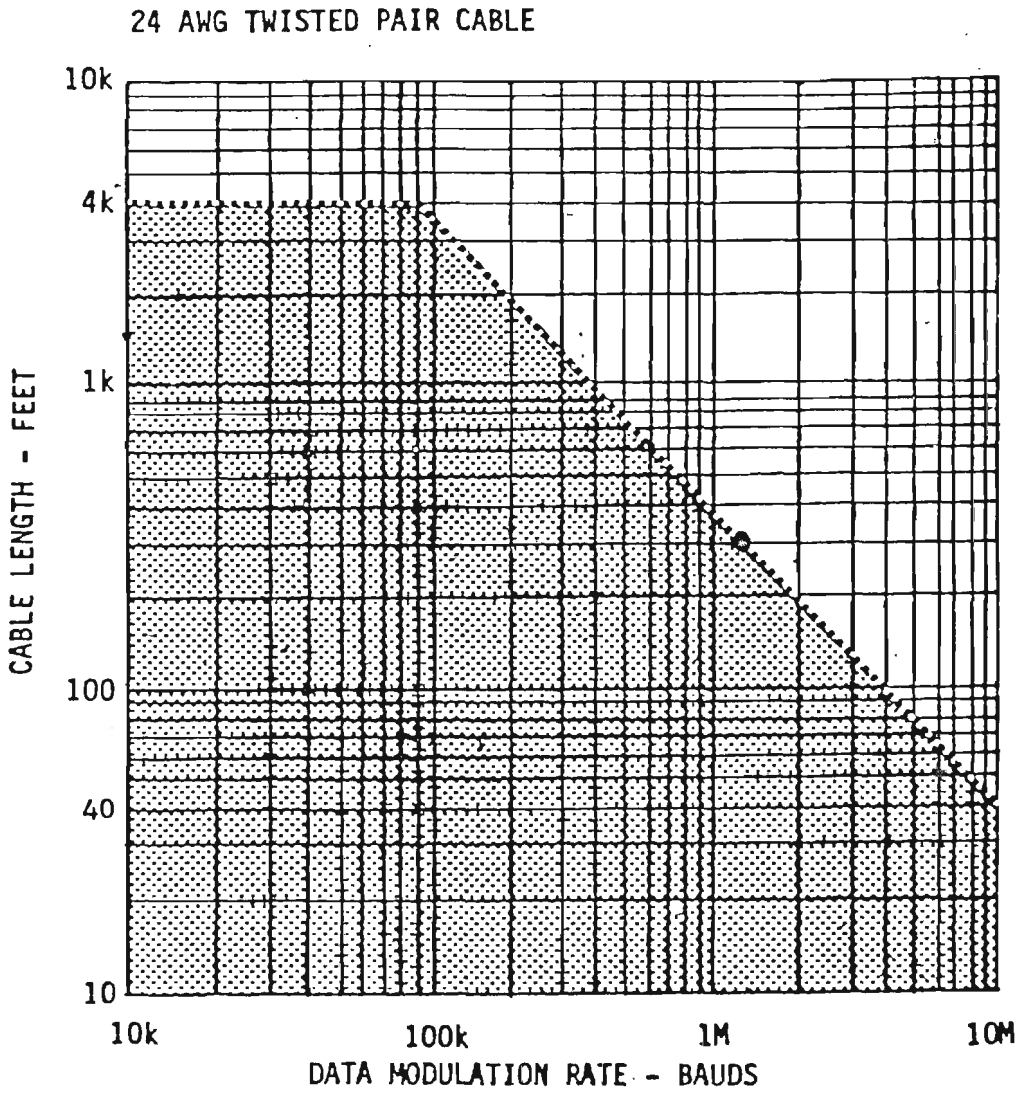

FIGURE 7.1

Data Modulation Rate Versus
Cable Length for Balanced Interface

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The curve of cable length versus modulation rate given in Figure 7.1 may be used as a conservative guide. This curve is based upon empirical data using a 24 gauge twisted-pair telephone cable terminated in a 100 ohm resistive load. The cable length restriction shown by the curve is based upon assumed load signal quality requirements of:

a. Signal rise and fall time equal to, or less than one-half unit interval at the applicable modulation rate.

b. A maximum voltage loss between generator and load of 6dBV.

At the higher modulation rates (0.09 to 10 megabauds) the sloping portion of the curve shows the cable length limitation established by the assumed signal rise and fall time requirements. As the modulation rate is reduced below 90 kilobauds, the cable length has been limited at 4000 feet by the assumed maximum allowable 6dBV signal loss.

The user is cautioned that the curve given in Figure 7.1 does not account for cable imbalance, or common mode noise beyond the limits specified that may be introduced between the generator and load by exceptionally long cables. On the other hand, while signal quality degradation within the bounds of Figure 7.1 will ensure a zero crossing ambiguity of less than .05 unit interval, many applications can tolerate greater timing and amplitude distortion. Thus correspondingly greater cable lengths may be employed than those indicated. Experience has shown that in most practical cases the operating distance at lower modulation rates may be extended to several miles.

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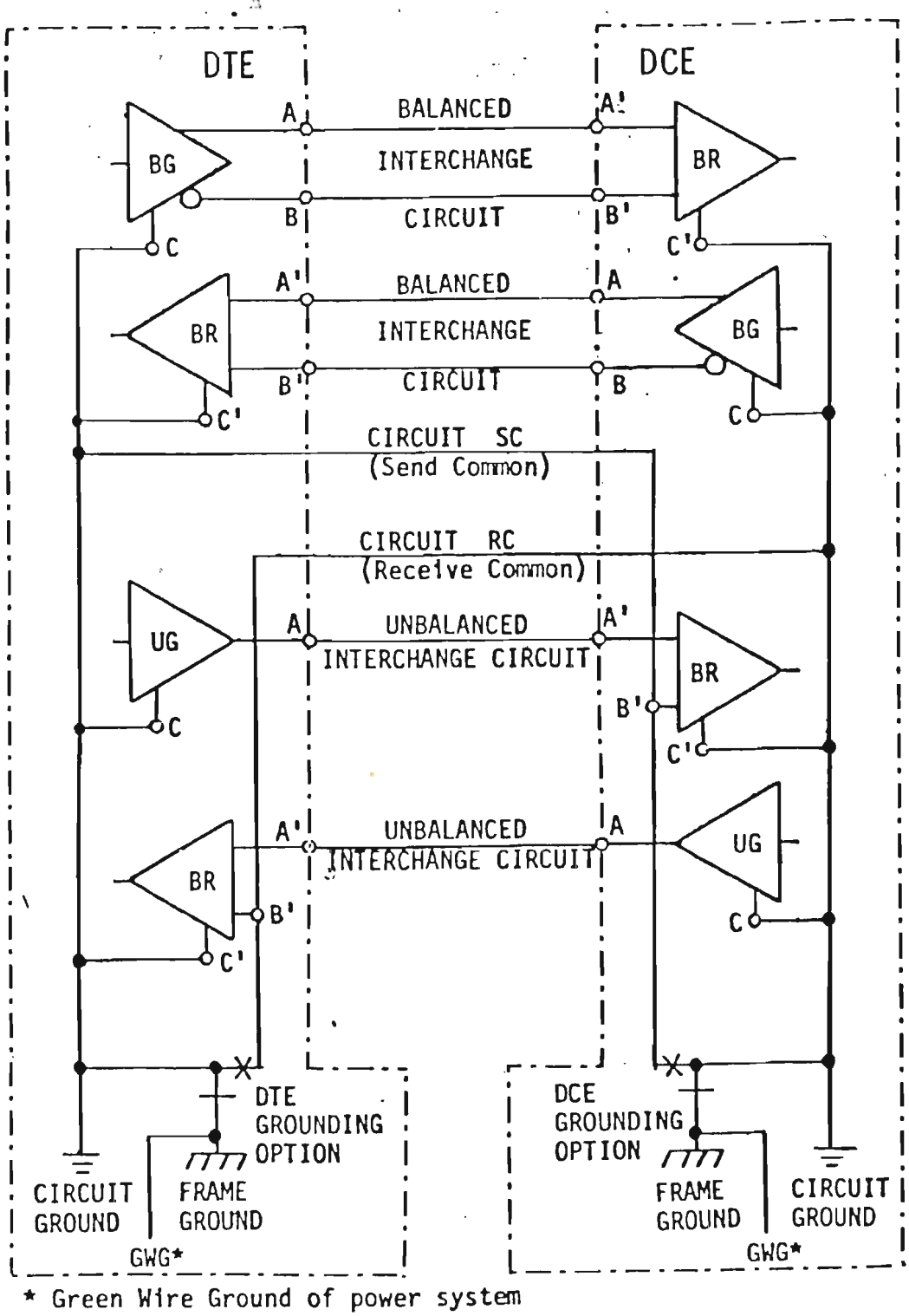
7.1.2 Cable Termination The characteristic impedance of twisted pair cable is a function of frequency, wire size and type as well as the kind of insulating materials employed. For example, the characteristic impedance of average 24 gauge, copper conductor, plastic insulated twisted pair telephone cable, to a 100 kHz sine wave will be on the order of 100 ohms.

In general, reliable operation of the balanced interface circuit is not particularly sensitive to the presence or absence of the cable termination at lower speeds (below 200 kilobaud) or at any speed where the signal rise time at the load end of the cable is greater than 4 times the one-way propogation delay time of the cable. At other speeds and distances, where signal reflections are of negligible significance, terminating the cable with a resistor ranging in value from 90 to 150 ohms tends to preserve generated signal rise time but at the expense of signal amplitude. At lower modulation rates, where zero crossing ambiguity and signal rise time are not critical, the cable need not be terminated.

7.2 Compatibility With Other Interfaces

The electrical characteristics of the balanced voltage digital interface are designed to allow use of both balanced and unbalanced (See RS-423) circuits within the same interconnection cable sheath. For example, the balanced circuits may be used for data and timing while the unbalanced circuits may be used for low speed control functions. The balanced interface circuit is not intended for



* Green Wire Ground of power system

FIGURE 7.2

Optional Grounding Arrangements

interoperation with other interface electrical characteristics such as RS-232-C, RS-423, MIL-STD-188C, and CCITT Recommendations V.28 and V.35. Under certain conditions with circuits of some of the above interfaces may be possible but may require modification in the interface or within the equipment, therefore, satisfactory operation is not assured and additional provisions not specified herein may be required.

7.3 Optional Grounding Arrangements

Proper operation of the interface circuits, whether using balanced, unbalanced, or a combination of electrical characterisitcs, requires the presence of a path between the circuit grounds of the equipments at each end of the interconnection. For example, in a DTE/DCE interface as shown in Figure 7.2, this path may be obtained in a number of ways:

a. Through Earth Ground. In this case, both end equipments have their circuit ground connected to frame ground which in turn is connected to earth ground (e.g., through the third wire (GWG) of the power cord). This is the preferred arrangement when the two earth grounds are at a potential difference of less than four volts.

b. By connecting Circuit SC (Send Common) to DCE circuit ground by means of a wiring option in the DCE. To avoid circulating ground currents, circuit ground must be separated from frame ground in the DCE when this connection is made. Thus, circuit ground for the DCE is obtained from the DTE circuit ground through the interchange circuit SC. The DCE must be capable of withstanding the resulting ground potential differences between its circuit ground and its frame ground. This is the preferred arrangement when the two earth grounds are at a potential difference greater than four volts and the DTE earth ground is the "quieter" of the two earth grounds.

c. By connecting Circuit RC (Receive Common) to DTE circuit ground by means of a wiring option in the DTE. To avoid circulating ground currents, circuit ground must be separated from frame ground in the DTE when this connection is made. Thus, the circuit ground for the DTE is obtained from the DCE circuit ground through interchange Circuit RC. The DTE must be capable of withstanding the resulting ground potential differences between its circuit ground and its frame ground. This is the preferred arrangement when the two earth grounds are at a potential difference greater than four volts and the DCE earth ground is the "quieter" of the two earth grounds.

6.2 - CARACTERÍSTICAS DAS PASTILHAS 75157 e 75159

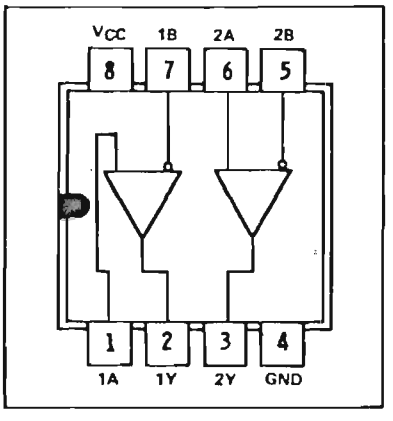
FUTURE PRODUCT
TO BE ANNOUNCED

TYPES SN55157, SN75157
DUAL DIFFERENTIAL LINE RECEIVERS

JANUARY 1977

- Meet EIA Standards RS-422 and RS-423
- Operates from a Single 5-V Supply
- Wide Common-Mode Voltage . . . ±15 V
- Standard V_{CC} and Ground Pin Positions
- Withstands EIA Standard RS-232-C Single Levels

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN55157 and SN75157 are dual differential line receivers that meet EIA Standards RS-422 and RS-423. They have the same features as the uA9637 but with standard V_{CC} and ground pin positioning.

The SN55157 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN75157 will be characterized for operation from 0°C to 70°C.

supply voltage: 5 V nominal

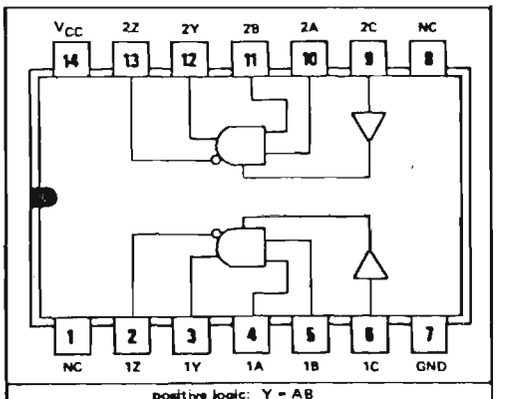
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPE SN75159
DUAL DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7712501, JANUARY 1977

- Meets EIA Standard RS-422
- Single 5-V Supply
- Balanced Line Operation
- TTL and DTL Compatible
- High-Impedance Output State for Party-Line Applications
- High-Current Active-Pull-Up Outputs
- Short-Circuit Protection
- Dual Channels
- Clamp Diodes at Inputs

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



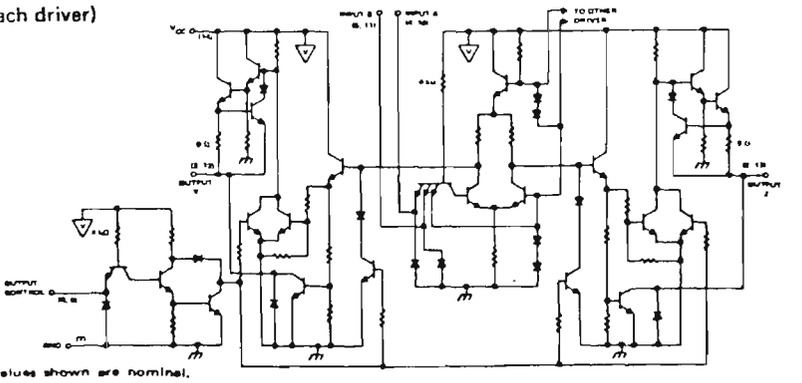
positive logic: $Y = AB$
$Z = \overline{AB}$
Outputs are off when C is low

NC—No internal connection

description

The SN75159 dual differential line driver with three-state outputs is designed to provide all the features of the SN75158 line driver with the added feature of driver output controls. There is an individual control for each driver. When the output control is low, the associated outputs are in a high-impedance state and the outputs can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

schematic (each driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state voltage applied to open-collector outputs	12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES. 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 18. In the J package SN75159 chips are glass-mounted.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−40	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OH} = −40 mA		2.4	3.0		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OL} = 40 mA			0.25	0.4	V
V_{OK}	Output clamp voltage	V_{CC} = MAX,	I_O = −40 mA			−1.1	−1.5	V
V_{OD1}	Differential output voltage	V_{CC} = MAX,	I_O = 0			3.5	$2V_{OD2}$	V
V_{OD2}	Differential output voltage	V_{CC} = MIN	R_L = 100 Ω,	See Figure 1	2	3.0		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage §	V_{CC} = MIN				0.02	0.4	V
V_{OC}	Common-mode output voltage ¶	V_{CC} = MAX				1.8	3	V
		V_{CC} = MIN				1.5	3	
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage §	V_{CC} = MIN or MAX				0.01	0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			0.1	100	μA
			V_O = −0.25 V			−0.1	−100	
			V_O = −0.25 V to 6 V				±100	
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX, Output controls at 0.8 V	T_A = 25°C,	V_O = 0 to V_{CC}			±10	μA
			T_A = 70°C	V_O = 0			−20	
				V_O = 0.4 V			±20	
				V_O = 2.4 V			±20	
				V_O = V_{CC}			20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1	−1.6	mA
I_{OS}	Short-circuit output current #	V_{CC} = MAX			−40	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, T_A = 25°C	Inputs grounded,	No load,		47	65	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at T_A = 25°C and V_{CC} = 5 V except for V_{OC}, for which V_{CC} is as stated under test conditions.
§$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶In EIA Standard RS-422, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
#Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF,	R_L = 100 Ω,	See Figure 2,		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output	Termination A				11	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	See Figure 2,	Termination B		13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					9	15	ns
t_{TLH}	Transition time, low-to-high-level output	C_L = 30 pF,	R_L = 100 Ω,	See Figure 2,		4	20	ns
t_{THL}	Transition time, high-to-low-level output	Termination A				4	20	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF,	R_L = 180 Ω,	See Figure 3		7	20	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF,	R_L = 250 Ω,	See Figure 4		14	40	ns
t_{PHZ}	Output disable time from high level	C_L = 30 pF,	R_L = 180 Ω,	See Figure 3		10	30	ns
t_{PLZ}	Output disable time from low level	C_L = 30 pF,	R_L = 250 Ω,	See Figure 4		17	35	ns
	Overshoot factor	R_L = 100 Ω,	See Figure 2,	Termination C			10	%

PARAMETER MEASUREMENT INFORMATION

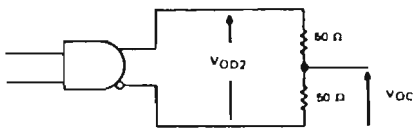
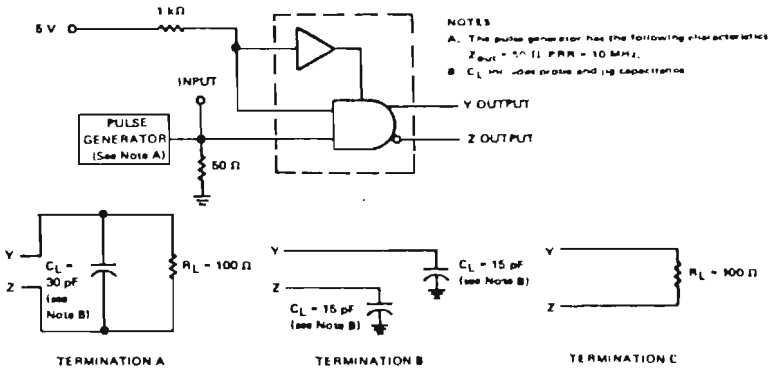
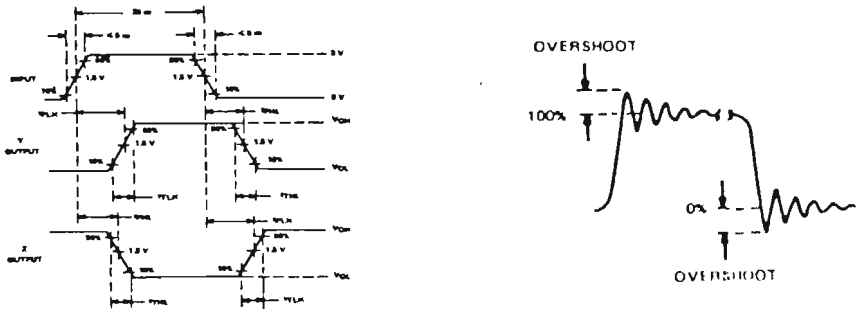


FIGURE 1—DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



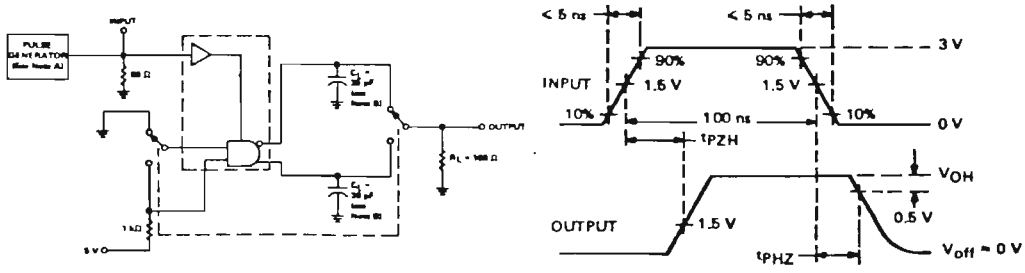
TEST CIRCUITS



VOLTAGE WAVEFORMS

FIGURE 2—t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, AND OVERSHOOT FACTOR

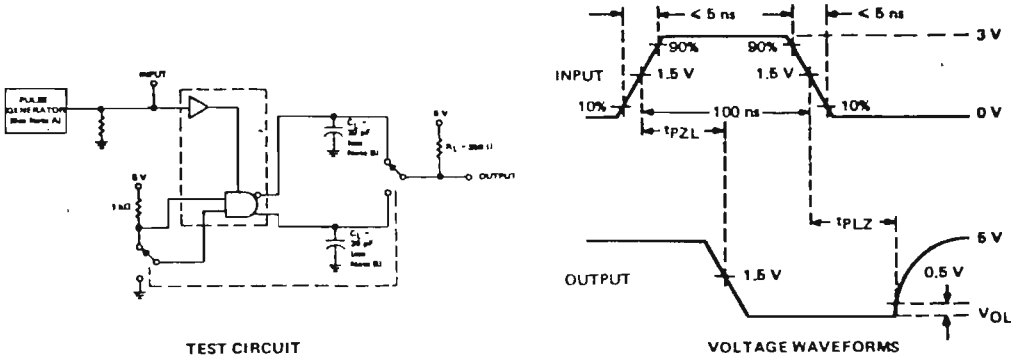
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

FIGURE 3—t_{PZH} AND t_{PHZ}



TEST CIRCUIT

VOLTAGE WAVEFORMS

FIGURE 4—t_{PZL} AND t_{PLZ}

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, PRR = 500 kHz
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

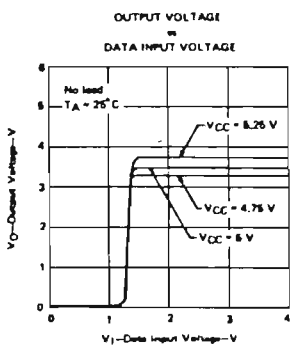


FIGURE 5

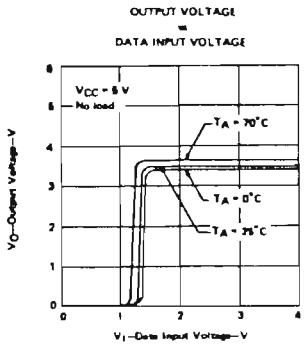


FIGURE 6

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TYPICAL CHARACTERISTICS

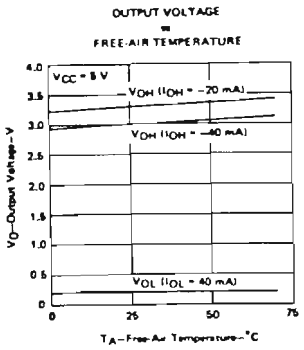

FIGURE 7

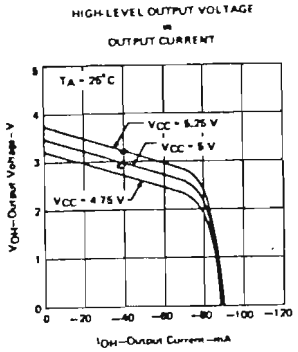

FIGURE 8

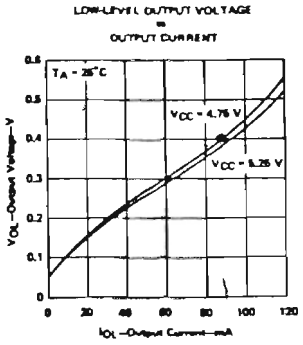

FIGURE 9

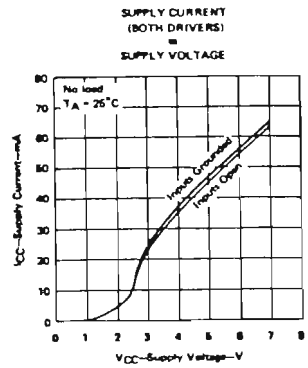

FIGURE 10

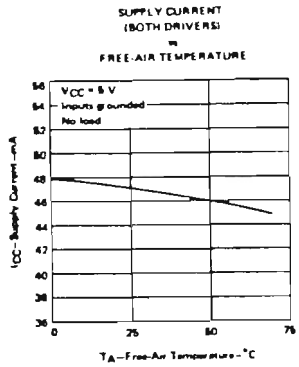

FIGURE 11

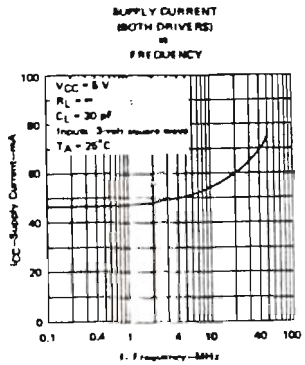

FIGURE 12

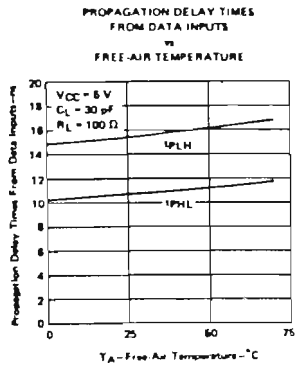

FIGURE 13

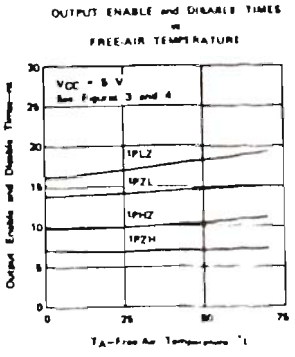

FIGURE 14